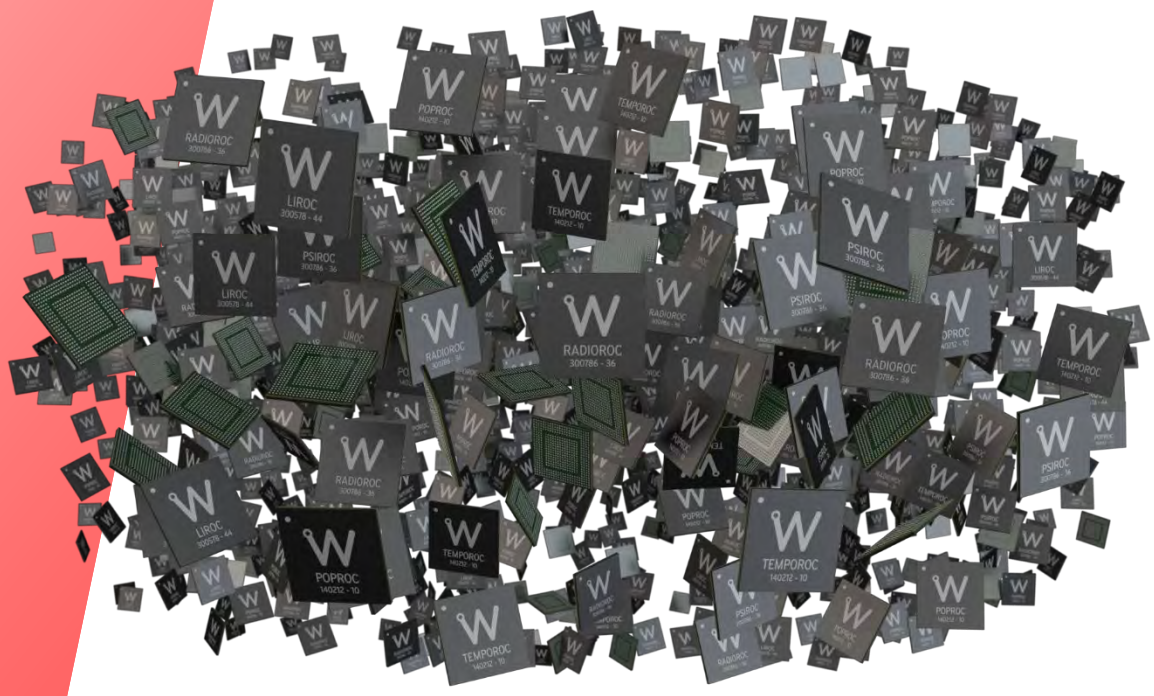
CAEN
Tools for Discovery

weeroc

High-end Microelectronics Design

Read-Out Chip Catalog



We are proud of the high quality of our products.

ISO 9001

ISO 9001:2015 approved quality system ensures all our internal processes.

From R&D to the registration of the incoming purchase orders, through:
- Resource Planning
- Scheduling
- Production

Our quality system is responsible for the proper functioning of all our internal processes and is subject to regularly audits, carried out by the National Standards Authority.

From the initial product design and its development stages, till the delivery of the production batches, we follow documented procedures that cover every aspect of our business.

The quality of CAEN S.p.A. products is constantly monitored by the application of the UNI EN ISO 9001:2015 standard. CAEN S.p.A. is ISO 9001 certified since 1998.

ISO9001:2015
certified Company

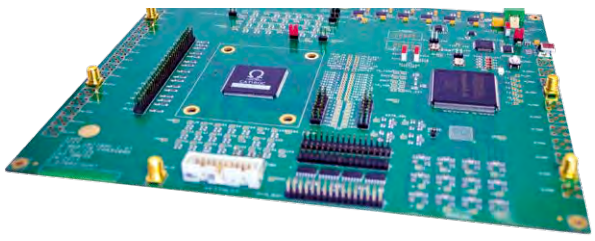
Authorised research laboratory of the MIUR

MORE INFO

WEEROC

FRONTEND ASICS FOR PARTICLE PHYSICS

CAEN carries the worldwide distribution agreement with Weeroc, the microelectronics company designing front-end readout ASICs for many photodetectors commonly used in physics applications. Weeroc offers a complete range programmable readout chips and associated support for a fast and succesfull integration in the final system.



Testboard

For each of the available ASIC, Weeroc offers a testboard designed to test and characterize the chip. This tool is suited to easily evaluate the performances of the ASIC and, thanks to its features, allows a versatile use with real detectors.

Product lineup

About Weeroc

Weeroc is a fabless microelectronics company designing and providing front-end read-out chips for most of the particle detector or photodetectors. Weeroc offers off-the-shelf programmable read-out chips and associated support for a fast and successful integration of the read-out chip in user system.

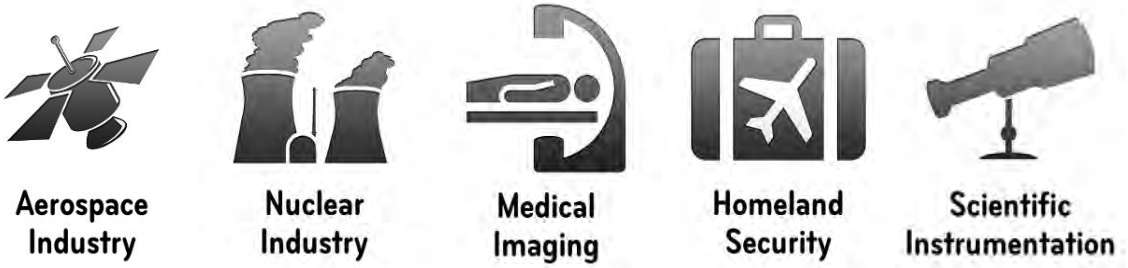
Weeroc designs custom read-out chip on customer request for specific application not covered by programmable component off the shelf.

Weeroc's core of design expertise includes low noise and radiation-hardened mixed signal ASICs.

Weeroc is certified ISO9001 since 2015.

Application Domains

Weeroc ASICs are suitable for most industrial or research application involving photodetector or particle detector read-out.

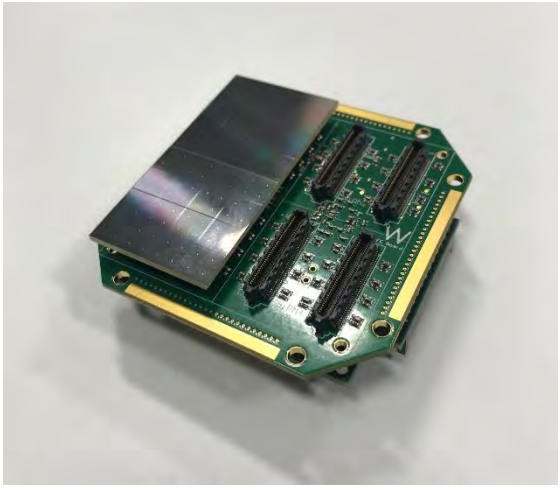


Dedicated Design

Weeroc can design dedicated ASIC for specific application. Non-recurrent design cost are paid by the final customer who have exclusive access to the design he ordered. Typical microelectronics design is 18 months from requirement specification to tested prototypes.

Integration services

Weeroc provide a dedicated front-end board design service to help our customer build their system if no system of the shelf meet their requirements.



Product lineup

Programmable read-out chip off the shelf

Weeroc offer a full range of product to read-out almost any kind of detectors. The table below describes which read-out chip is suitable for which kind of detectors. Weeroc application engineers can help you choose the best fit for your detector and application.

	SiPM	MA-PMT / MCP-PMT	PMT	APD	Pin diode	Silicon strips	RPCs	Micromegas GEMS
Maroc 3A	✓	✓	✓					
Catiroc 1	✓	✓	✓					
Poproc	✓	✓	✓					
Citiroc 1A	✓							
Petiroc 2A	✓						✓	
Triroc 1A	✓							
Liroc2	✓						✓	
Radioroc2	✓						✓	
Temporoc2	✓							
Skiroc 2A				✓	✓	✓		
Psiroc				✓	✓	✓	✓	✓
Gemroc 1								✓

Weeroc products maturity is ranged using technical readiness level (TRL) scale. The Weeroc definition of TRL is described below.

Technology Readiness Level	Description
TRL 1	ASIC project
TRL 2	ASIC in foundry
TRL 3	silicon available
TRL 4	First measurements, minor bug detected
TRL 5	First measurement, conclusive in lab
TRL 6	Application prototype available
TRL 7	Full system using ASIC available
TRL 8	Full system using ASIC running
TRL 9	Full system running ASIC, reliability proven

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	Maroc	Catiroc	Gemroc	Skiroc	Citiroc
Prod. Version	3A	1	1	2A	1A
TRL	9	8	9	8	9
Package*	PQFP240 TFBGA353	TQFP208	PQFP160	BGA400	PQFP160 TFBGA353
Detector Compatibility	- MA-PMT, PMT - SiPM, SiPM array	- MA-PMT, PMT	- micromegas - GEMs	- Si PIN diodes - Silicon strips	- SiPM - SiPM array
Channel	64	16	64	64	32
Measurements and operations	- Free running trigger - External trigger - Charge (shaper) - Photon counting - Time (trigger)	- Free running trigger - External trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - External trigger - Charge (shaper) - Data 3-level trigger	- Free running trigger - External trigger - Charge (shaper) - Time (TDC)	- Free running trigger - External trigger - Charge (shaper) - Time (trigger)
Outputs	- 64 Triggers - Trigger OR - 1 analog multi-plexer (charge) - ADC (8/10/12-bit)	- 16 Triggers - 16 Shapers - Trigger OR - ADC (10-bit) - TDC (10-bit)	- Trigger OR - 1 analog multi-plexer (charge)	- Trigger OR - 1 analog multi-plexer (charge) - ADC (10/12 bit) - TDC (10/12 bit)	- 32 triggers - Trigger OR - 1 analog multi-plexer (charge)
Input Polarity	Negative	Negative	Negative	Positive	Positive
Applications **Main features**	- Energy meas. - SPE application - Photon counting rate < 30MHz - MA-PMT gain adj.	- Energy meas. - Time stamping - Low dead time - Zero suppress data	- Energy meas. - Time stamping - Data readout: 3-level trigger	- Energy meas. - Time stamping	- Energy meas. - Time of flight - Photon counting - Calibration input - SPE spectrum - Input DAC - SiPM HV adjust.

** QFP packaging will be phased out and replaced with equivalent BGA packaging.*

*** BGA516 20x20mm2 – Pin-to-pin compatible*

Glossary: ADC : Analog to Digital Converter – TDC : Time to Digital Converter

Product lineup

Petiroc	Triroc	Radioroc NEW	Psiroc NEW	Liroc NEW	Temporoc NEW	PopRoc NEW
2A	1A	2	1	1	2	1
6	8	4	4	4	4	4
TQFP208 TFBGA353	TFBGA353	BGA516**	BGA516**	BGA516**	BGA516**	BGA516
- SiPM - SiPM array	- SiPM - SiPM array	- SiPM - SiPM array	- PIN Diodes, - Silicon strips, - GEMs	- SiPM - SiPM array	- SiPM - SiPM array	- SiPM - SiPM array
32	64	64	64	64	64	
- Free running trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Charge (shaper) - Time (TDC)	- Free running trigger - External trigger -Charge (shaper, ToT) - Time & Charge (trigger) - Photon Counting	- Free running trigger - External trigger Charge (shaper, ToT) - Time (trigger)	- Free running trigger - Time (trigger) - Photon Counting - Charge (ToT)	- Free running trigger - Charge (shaper) - Time (TDC)	- Free running trigger - Time (trigger) - Photon Counting - Charge (ToT)
- 32 triggers - Trigger OR - 1 analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10 bit) - TDC (10 bit)	- Trigger OR - analog multiplexer (charge) - 1 digital multiplexer (trigger) - ADC (10 bit) - TDC (10 bit)	- Selectable per channel: • 1 LVDS trigger • 2 single ended trigger • 2 shaper outputs - 3 triggers NOR - 2 analog MUX	- Selectable per channel: • 1 LVDS trigger • 2 single ended trigger • 2 shaper outputs - 3 triggers NOR - 2 analog MUX	- 64 LVDS trigger outputs	- Trigger OR - Analog MUX (charge) - Digital MUX (trigger) - ADC (10-bit) - TDC (50 ps)	- 64 LVDS trigger outputs
Negative (optimized) Positive	Negative (optimized) Positive	Positive	Positive (optimized), negative	Positive, negative	Positive	Positive (optimized), negative
- Energy meas. - Time of flight - Time stamping - Photon counting - Input DAC - SiPM HV adjust.	- Energy meas. - Time of flight - Time stamping - Zero suppress data - Input DAC - SiPM HV adjust.	- Energy meas. - Time of flight - Photon counting ~200MHz - Dual time thresholds - SPE spectrum - SiPM HV adjust.	- Energy meas.	- Time of flight - Photon counting ~300MHz - SPE spectrum - Energy meas. - SiPM HV adjust.	- Energy meas. - Time of flight - Time stamping - SiPM HV adjust.	- Time of flight - Photon counting ~300MHz - SPE spectrum - Energy meas. - SiPM HV adjust.

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Maroc 3A

Photomultiplier-tubes read-out chip

MAROC3A is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron (50fC) and a charge measurement up to 30 photoelectrons (~ 5 pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 4 thanks to an 8-bit variable gain preamplifier allowing to compensate the non- uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5 pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths: one made of a bipolar or unipolar fast (15 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1 pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit Wilkinson ADC.

Detector Read-Out	MAPMT, SiPM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron with a 10^6 PM gain or 50 fC
Timing Resolution	60ps RMS on single photo-electron, threshold 1/3 of photo-electron
Dynamic Range	5 pC (10^6 PM gain), Integral Non Linearity: 2% up to 5 pC
Packaging & Dimension	TFBGA353, ~~PQFP240~~ discontinued
Power Consumption	3.5 mW /ch, power supply= 3.3V
Inputs	64 current inputs
Outputs	64 trigger outputs Wired OR of the 64 triggers for each of the 2 discriminators 1 multiplexed analog charge output that can be daisy chained 1 digital charge measurement (8, 10 or 12 bits)
Internal Programmable Features	gain adjustment between 0 and 2 over 8 bits for each input preamp, trigger threshold adjustment (10bits), analog and digital charge measurement, 64 trigger outputs, 64 trigger masks

They are using Maroc 3A

CERN (ATLAS luminometer)
Jefferson lab (CLASS12)
Industrial applications under NDA

More about Maroc 3A

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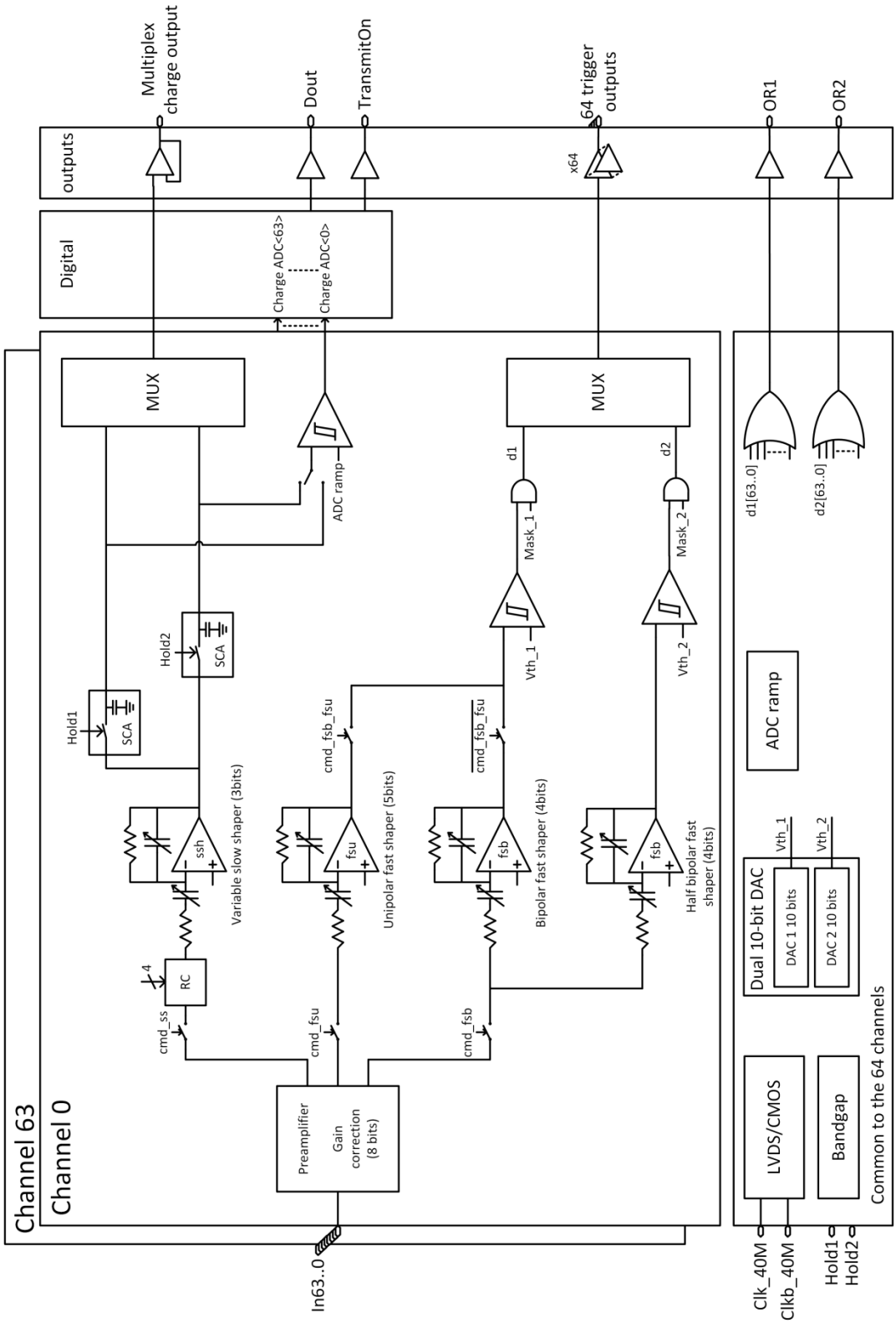
Multiplex charge output
Dout
TransmitOn
64 trigger outputs
OR1
OR2
outputs
x64
Digital
Charge ADC<63>
Charge ADC<0>
MUX
MUX
ADC ramp
d1
d2
Mask_1
Mask_2
Vth_1
Vth_2
d1[63..0]
d2[63..0]
Hold2
SCA
Hold1
SCA
cmd_fsb_fsu
cmd_fsb_fsu
ssh
fsu
fsb
fsb
Variable slow shaper (3bits)
Unipolar fast shaper (5bits)
Bipolar fast shaper (4bits)
Half bipolar fast shaper (4bits)
ADC ramp
Dual 10-bit DAC
DAC 1 10 bits
DAC 2 10 bits
Vth_1
Vth_2
4
RC
cmd_ss
cmd_fsu
cmd_fsb
Preamplifier
Gain correction (8 bits)
LVDS/CMOS
Bandgap
Common to the 64 channels
Channel 63
Channel 0
In63..0
Clk_40M
Clkb_40M
Hold1
Hold2

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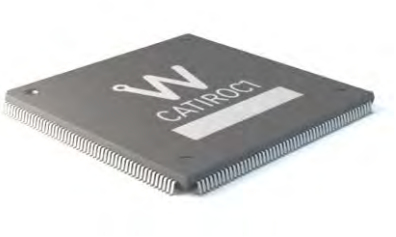
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip

CATIROC 1 is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs) in large scale applications such as water Cerenkov experiments. The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell for large area of detection.

An adjustment of the gain of each channel compensates for the gain variation of the PMTs and allows using only one HV cable for the 16 PMTs. In the ASIC, the 16 channels are totally independent. In each channel, the auto-trigger starts the charge and time measurements which are then converted and stored. Only the hit channels are read out by one serialized output. The time measurement is done by a 26-bit counter at 40 MHz for the coarse time and a Time to Amplitude Converter (TAC) for the fine time, giving a resolution of 200ps RMS. The charge measurement is done by a dual gain preamplifier followed by a shaper with variable shaping times (25 ns, 50 ns or 100 ns). Charge and fine time values are converted by a 10 bit ADC.

Moreover CATIROC 1 can be used as an analogue front-end ASIC for PMTs. The 16 triggers and 16 shapers output can be used in an application specific optimized front-end board.



Detector Read-Out	PMT, PMT array
Number of Channels	16
Signal Polarity	Negative
Sensitivity	Trigger on one third of photo-electron on each channel
Timing Resolution	200ps RMS on single photo-electron
Dynamic Range	400 photo-electrons (10^6 PMT gain) Integral Non Linearity 1% up to 400 p-e
Packaging & Dimension	TQFP208
Power Consumption	Power supply: 3.3V 21mW/ch.
Inputs	16 voltage inputs
Outputs	16 trigger outputs 16 shaper output 1 or of the 16 trigger output 1 serialized digital data output (50bits/channel)
Internal Programmable Features	16 channel gain adjustment (16x8bits), trigger and gain threshold adjustment (2x10bits), charge measurement tuning, 16 trigger masks, channel by channel trigger output enable.

They are using Catiroc 1

JUNO experiment
WA105 collaboration

More about Catiroc 1

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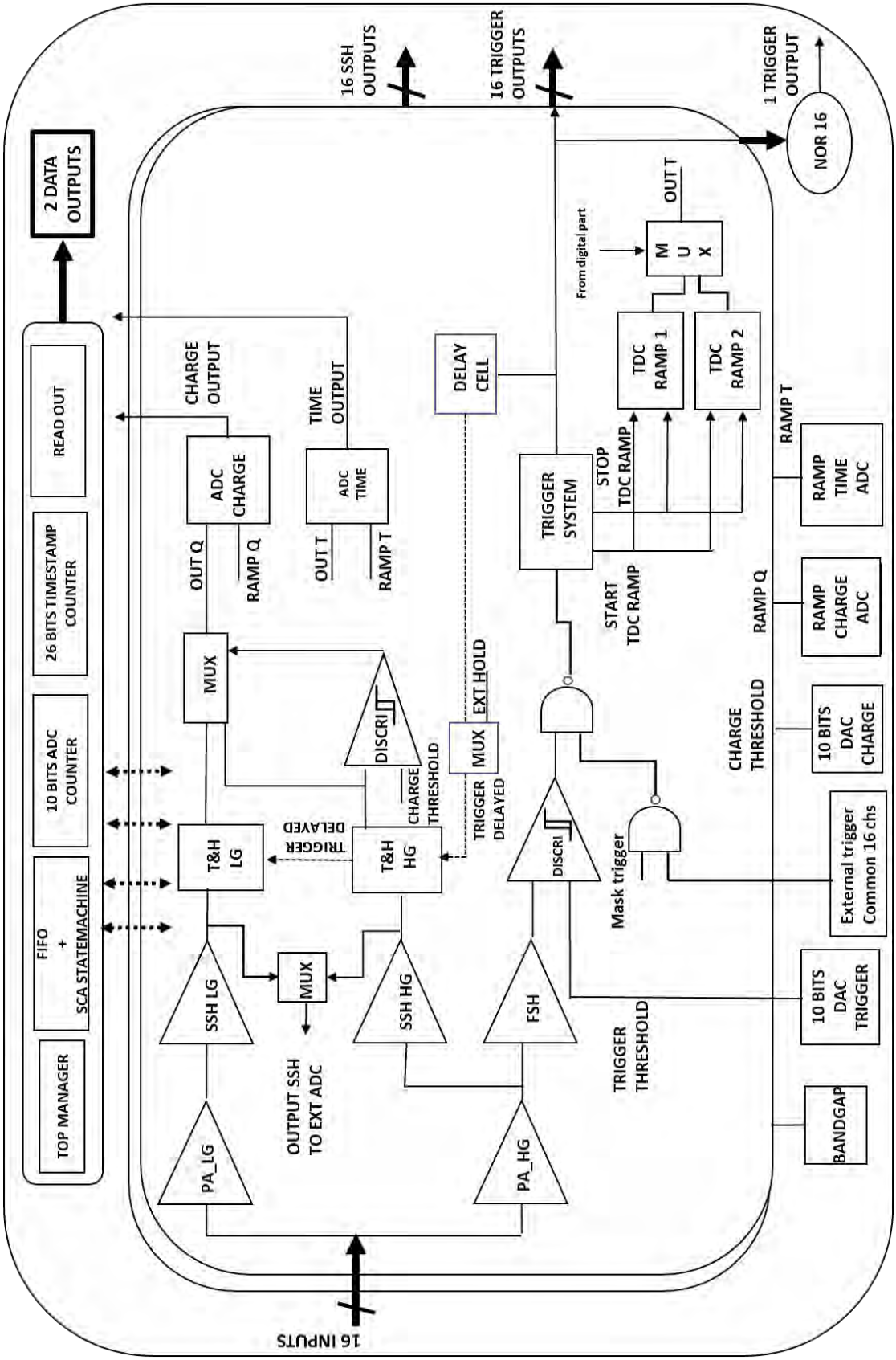
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip



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Citiroc 1A

Scientific instrumentation SiPM read-out chip

Citiroc 1A is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for scientific instrumentation application.

Citiroc 1A allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc 1A outputs the 32-channel triggers with a high accuracy (better than 100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs. Citiroc 1A can be calibrated using a unique calibration signal.

Timing measurement better than 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 p.e. The power consumption 225mW with all stages on.

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP 160 – TFBGA353
Power Consumption	225mW – Supply voltage : 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 2 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

They are using Citiroc 1A

INAF – IASF (CTA experiment)
INAF – ASTRI Camera
CERN (Baby mind experiment)

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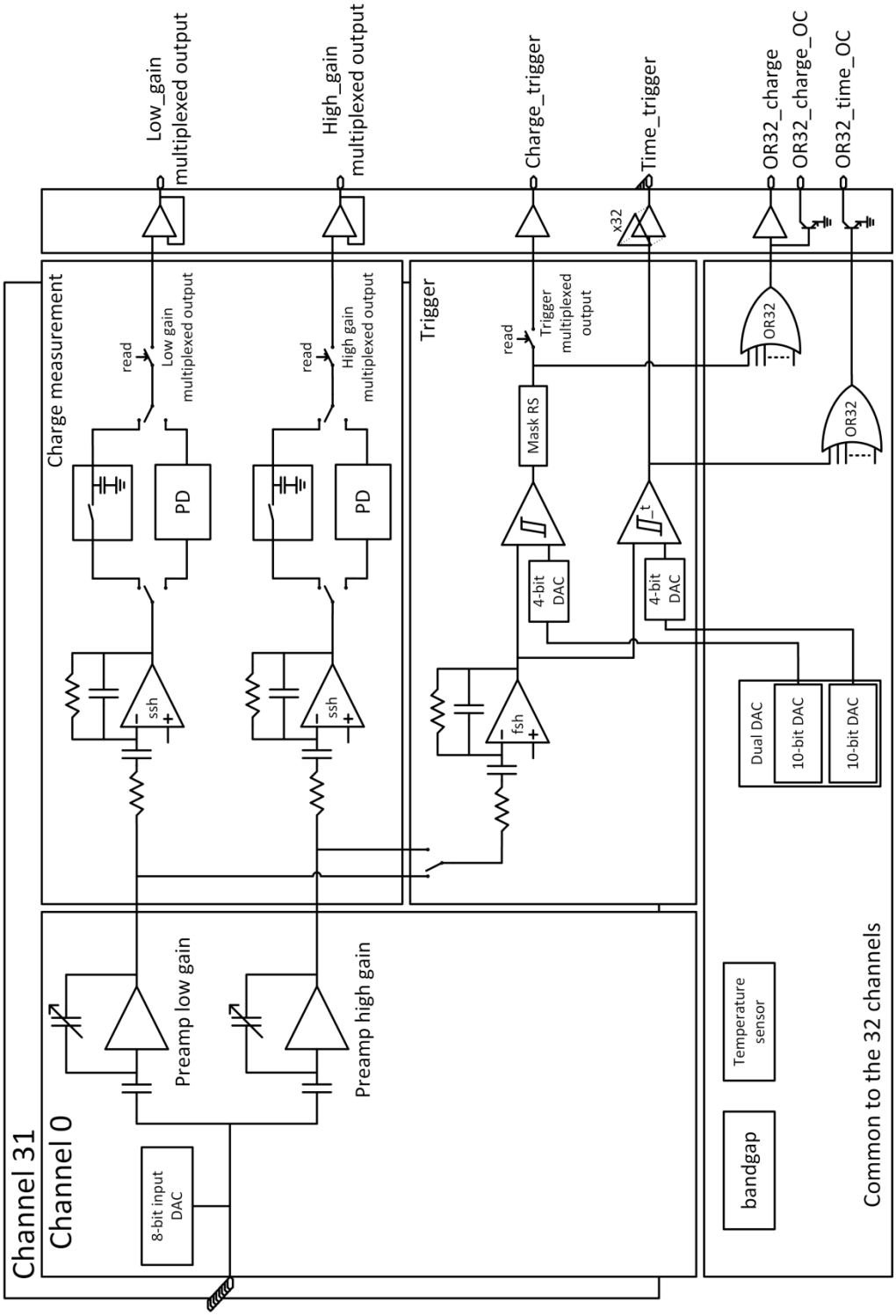
More about Citiroc 1A



SSH – Slow Shaper ; FSH – Fast Shaper; PD – Peak Detector

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Petiroc 2A

SiPM read-out for time-of-flight PET

Petiroc 2A is a 32-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Petiroc 2A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 40ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6 mW/channel, excluding buffers used to output the analogue signals. The main application of Petiroc 2A is PET time-of-flight prototyping but it can also be used for any application that requires both accurate time resolution and precise energy measurement.

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch

They are using Petiroc 2A

Industrial applications
Cannot be disclosed

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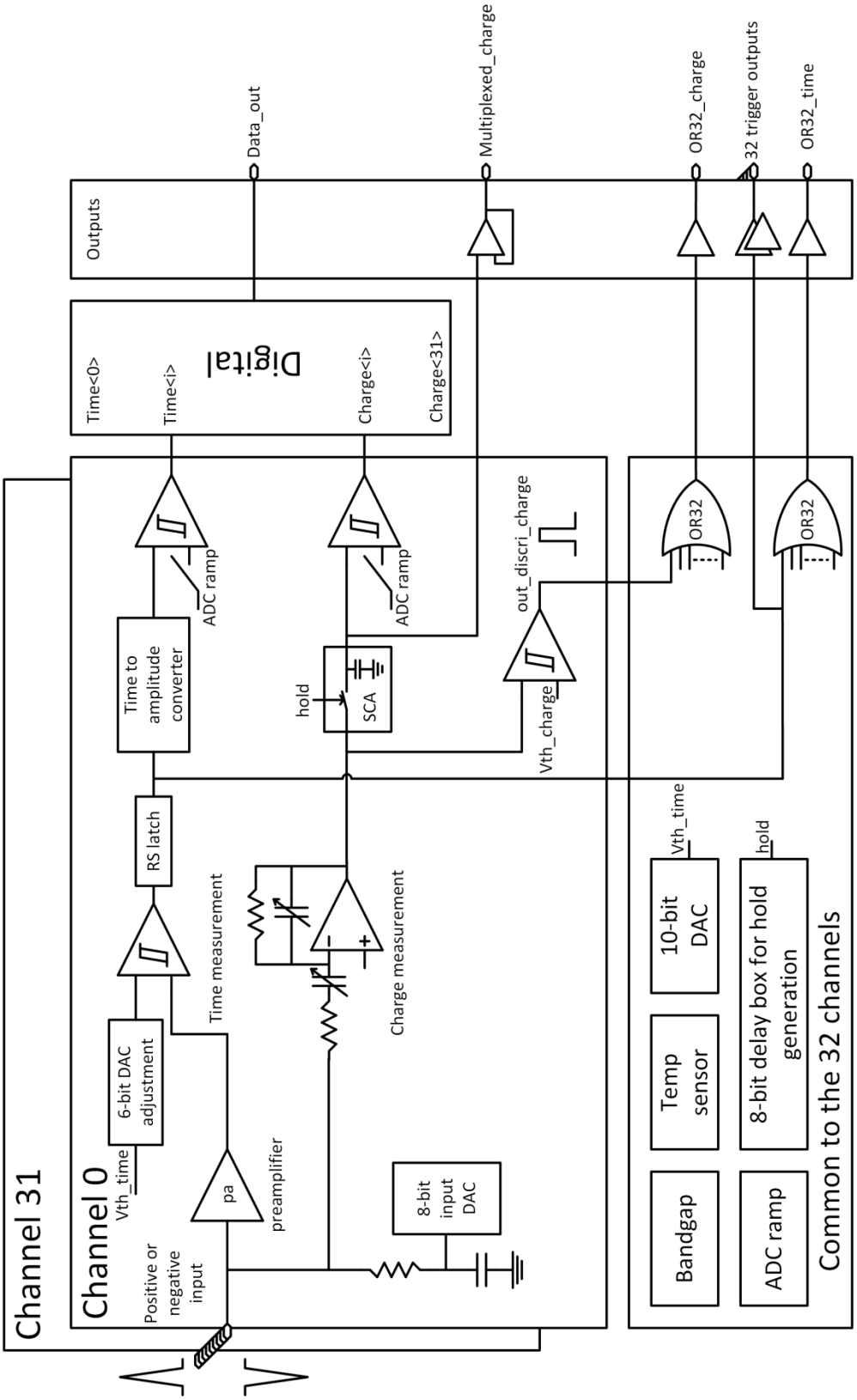
More about Petiroc 2


Data_out
Multiplexed_charge
OR32_charge
32 trigger outputs
OR32_time
Outputs
Digital
Time<0>
Time<i>
Charge<i>
Charge<31>
ADC ramp
ADC ramp
out_discri_charge
OR32
OR32
Time to amplitude converter
hold
SCA
Vth_charge
RS latch
Time measurement
Charge measurement
Vth_time
10-bit DAC
hold
6-bit DAC adjustment
Vth_time
pa
preamplifier
8-bit input DAC
Temp sensor
8-bit delay box for hold generation
Positive or negative input
Bandgap
ADC ramp
Channel 31
Channel 0
Common to the 32 channels

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Triroc 1A

All-in-one SiPM read-out for multimodal PET inserts

Triroc 1A is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Triroc 1A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 30ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. The main application of Triroc 1A is PET time-of-flight but it can also be used for any application that requires both accurate time resolution and precise energy measurement. Triroc 1A is available in naked dies or BGA packaging (12x12mm, 353 balls).

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, trigger latch, Power Pulsing

They are using Triroc 1A

Trimage collaboration (PET/IRM/EEG)
Industrial application
Cannot be disclosed

More about Triroc 1A

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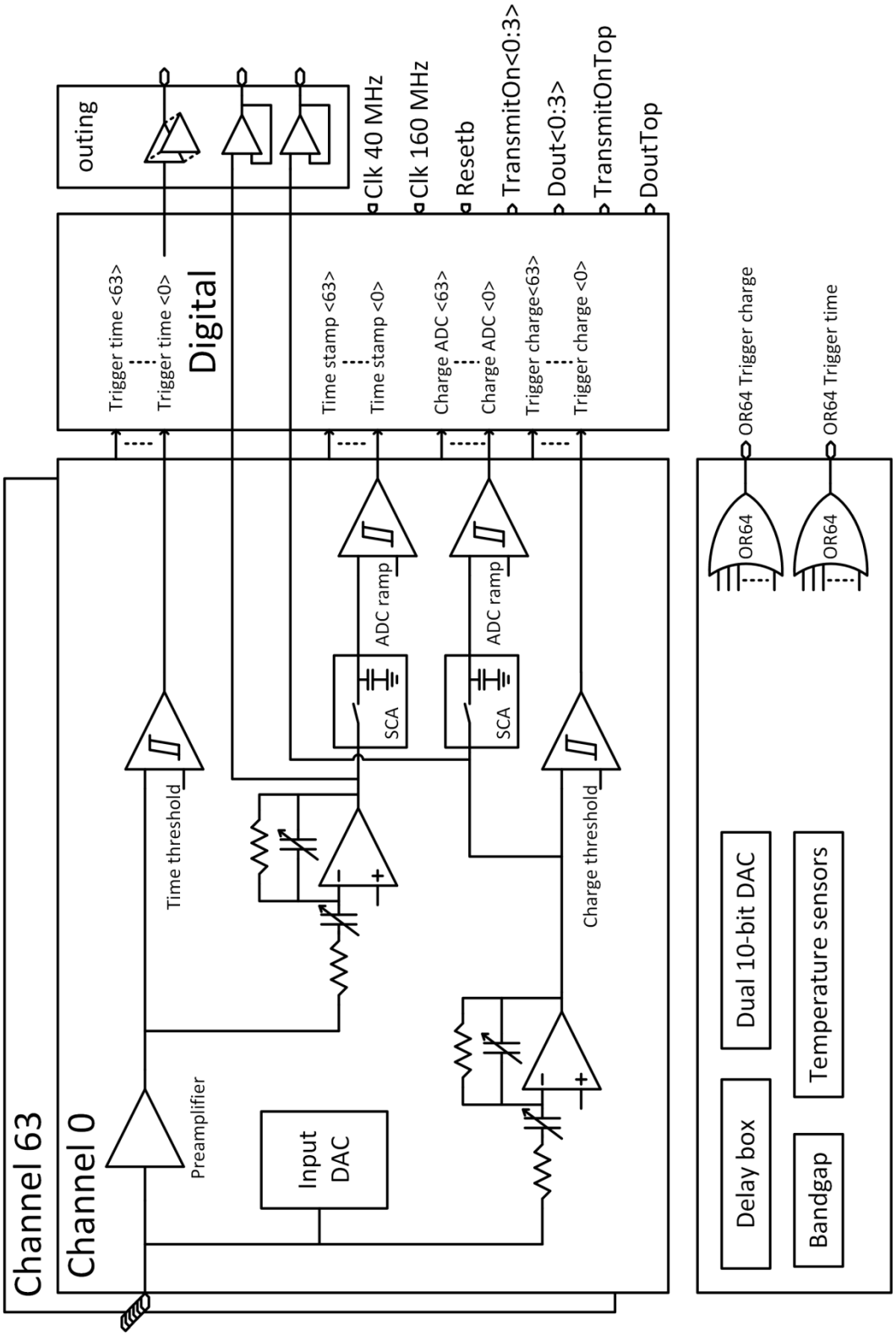
outing
Clk 40 MHz
Clk 160 MHz
Reset b
TransmitOn<0:3>
Dout<0:3>
TransmitOnTop
DoutTop
Digital
Trigger time <63>
Trigger time <0>
Time stamp <63>
Time stamp <0>
Charge ADC <63>
Charge ADC <0>
Trigger charge<63>
Trigger charge <0>
OR64 Trigger charge
OR64 Trigger time
OR64
OR64
ADC ramp
ADC ramp
SCA
SCA
Time threshold
Charge threshold
Preamplifier
Input DAC
Channel 63
Channel 0
Dual 10-bit DAC
Temperature sensors
Delay box
Bandgap

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Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip

SKIROC 2A is a 64-channel front-end ASIC designed to readout silicon PIN diodes. Each channel is made of a variable-gain and low-noise charge preamplifier followed by two shapers – one with a gain of 1 and the other with a gain of 10 – to provide a charge measurement from 0.2 fC up to 10 pC. A time tagging is performed by a 12-bit TDC ramp. The charges and times are stored in a 15-depth Switched Capacitor Arrays (SCA), the values of which are converted by a multi-channel 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The analog value of the charge is also available on an output pin. The trigger chain is composed of a high gain fast shaper and a discriminator and allows each channel to auto trigger down to 0.2 fC. Thresholds of the 64 discriminators are set by a common 10-bit DAC and an individual 4-bit DAC per channel. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns) to provide the Hold signal for the SCA cells of the slow channel. The power consumption is 6.2 mW/channel and each stage can be individually shut down when not used. 616 slow control parameters are available to set various configurations and ensure the versatility of the chip.

Detector Read-Out	Si PIN Diodes
Number of Channels	64
Signal Polarity	positive
Sensitivity	Trigger on 0.2fC
Timing Resolution	N/A
Dynamic Range	10 pC, Integral Non Linearity <1%
Packaging & Dimension	BGA 400 (17x17mm)
Power Consumption	6.2 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	1 multiplexed analog charge output 12-bit charge and time measurement Trigger OR of the 64 discriminators
Internal Programmable Features	Common gain adjustment for the input, common trigger threshold adjustment (10 bits) and individual threshold (4 b), 12-bit charge and time measurement, 64 trigger masks, multiplexed analog output

They are using Skiroc 2A

CALICE ECAL

More about Skiroc 2A

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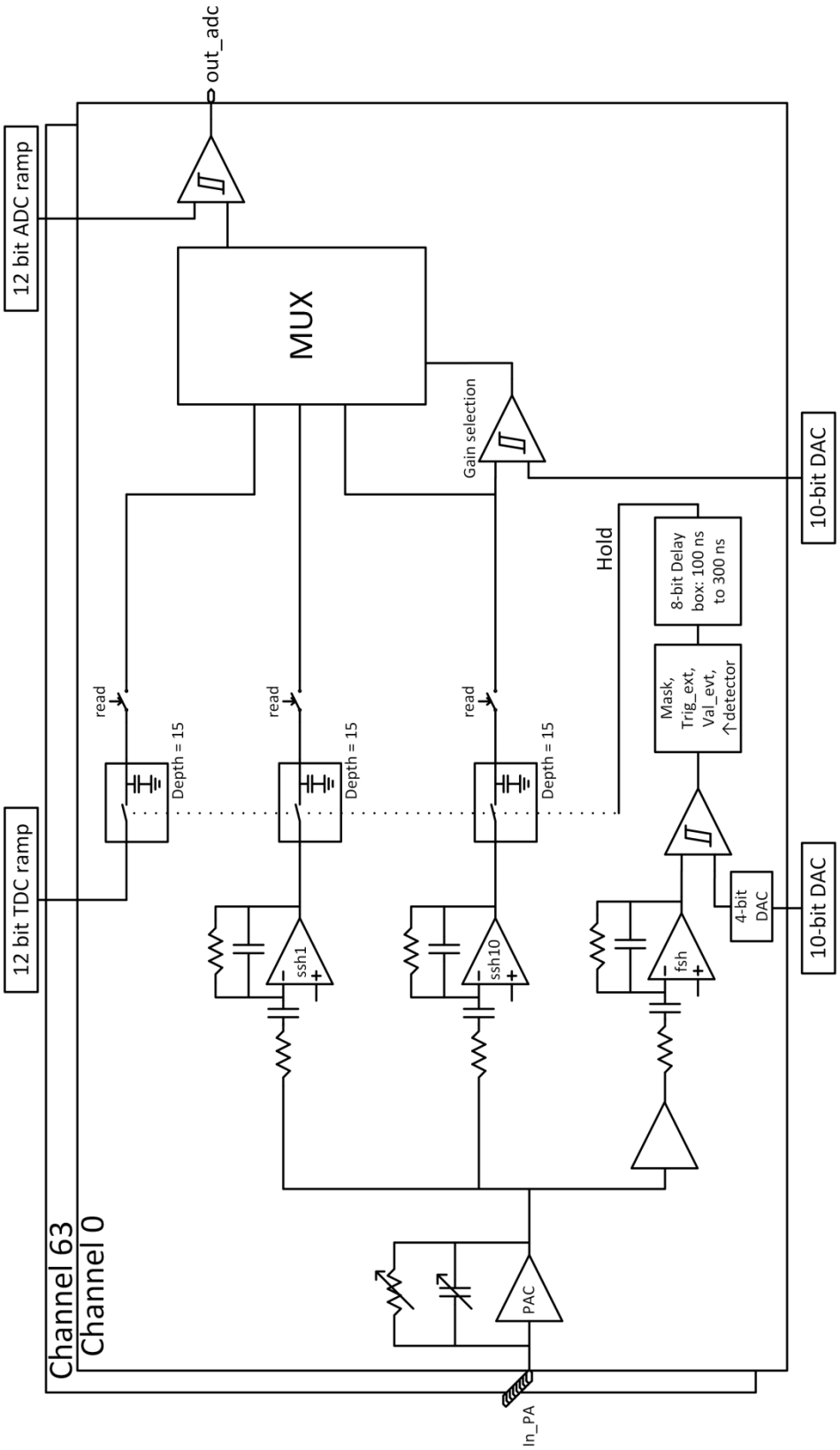
out_adc
12 bit ADC ramp
MUX
Gain selection
10-bit DAC
Hold
8-bit Delay box: 100 ns to 300 ns
Mask, Trig_ext, Val_evt, ↑detector
read
Depth = 15
12 bit TDC ramp
ssh1
ssh10
fsh
4-bit DAC
10-bit DAC
Channel 63
Channel 0
PAC
In_PA

weeroc

Gemroc 1

Micromegas and GEMs semi-digital read-out chip

GEMROC 1 is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from low gain detectors (GEMs, Micromegas, ...). GEMROC 1 provides a semi-digital readout with three thresholds tunable from 1 fC to 500 fC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the timestamp from a 24b counter. The three thresholds are set internally by three 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 1 fC input charge. A multiplexed charge measurement up to 500fC is integrated.

The power consumption is 1.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.

Detector Read-Out	Micromegas, GEM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger 1 fC
Timing Resolution	N/A
Dynamic Range	500 fC
Packaging & Dimension	TQFP160
Power Consumption	1.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	Trigger threshold adjustment (10bits), 3*64 trigger masks, multiplexed latched trigger or direct OR64 trigger outputs

They are using Gemroc 1

Industrial application (NDA)

More about Gemroc 1

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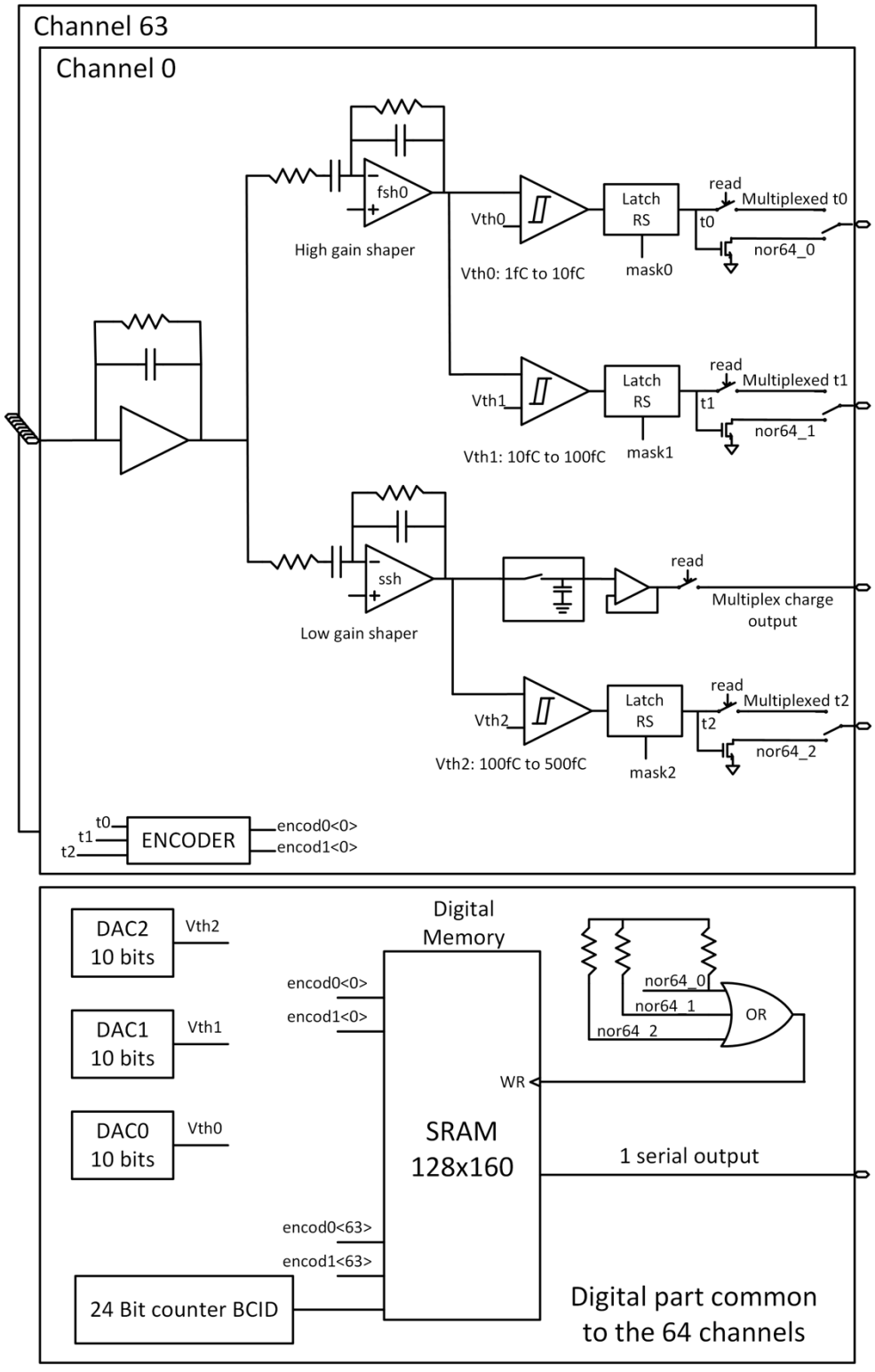

Channel 63
Channel 0
fsh0
High gain shaper
Vth0
Vth0: 1fC to 10fC
Latch RS
mask0
read
Multiplexed t0
t0
nor64_0
Vth1
Vth1: 10fC to 100fC
Latch RS
mask1
read
Multiplexed t1
t1
nor64_1
ssh
Low gain shaper
read
Multiplex charge output
Vth2
Vth2: 100fC to 500fC
Latch RS
mask2
read
Multiplexed t2
t2
nor64_2
t0
t1
t2
ENCODER
encod0<0>
encod1<0>
DAC2 10 bits
Vth2
DAC1 10 bits
Vth1
DAC0 10 bits
Vth0
Digital Memory
encod0<0>
encod1<0>
nor64_0
nor64_1
nor64_2
OR
WR
SRAM 128x160
1 serial output
encod0<63>
encod1<63>
24 Bit counter BCID
Digital part common to the 64 channels

weeroc

Poproc

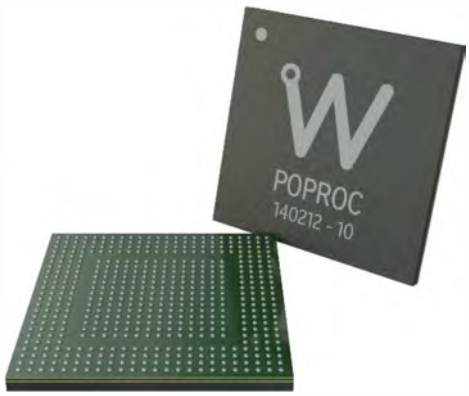
MA-PMT readout chip Photon Counting Application

POPROC is a MA-PMT readout out chip, specifically design for fast counting output. This chip is fully analog and features differential trigger output for each detector channel. The ASIC is designed to accept negative polarity input and can readout up to 64 channels.

POPROC allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 3 ns separated single photo-electrons). POPROC allows fast single photon counting over 300MHz per channel.

Channel-by-channel calibration on the trigger threshold is also possible thanks to 6-bit DACs.

POPROC features a GHz measurement line composed of a current conveyor followed by a fast discriminator and low swing differential output driver.



Detector Read-Out	PMT, MA-PMT
Number of Channels	64
Signal Polarity	Negative (selectable to work on Positive)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 3 ns double-peak separation on single photo-electron Over 300MHz photon counting rate
Dynamic Range	Over 100 photo-electrons
Packaging & Dimension	BGA 20x20 mm^2 Flip-Chip low inductance packaging technology
Power Consumption	210mW – Supply voltage: 1.2 V
Inputs	64 analogue inputs
Outputs	64 differential (CLPS) triggers
Internal Programmable Features (I^2C)	trigger threshold programming (10bits), 64 x 6-bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp bandwidth adjustment, individual trigger masking.

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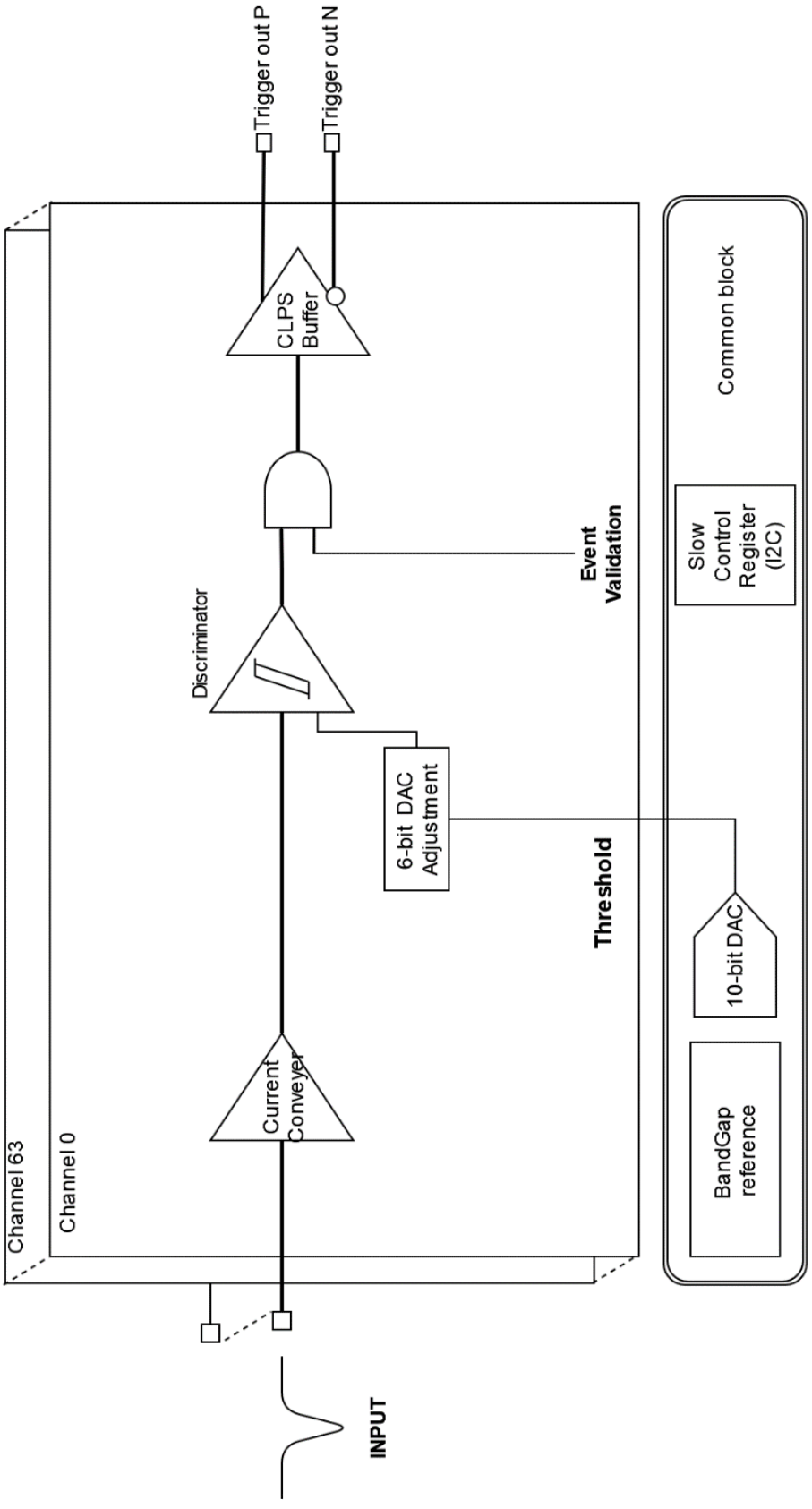
More about Poproc


Trigger out P
Trigger out N
CLPS Buffer
Event Validation
Discriminator
6-bit DAC Adjustment
Threshold
Current Conveyer
Channel 63
Channel 0
INPUT
Common block
Slow Control Register (I2C)
10-bit DAC
BandGap reference

weeroc

Liroc

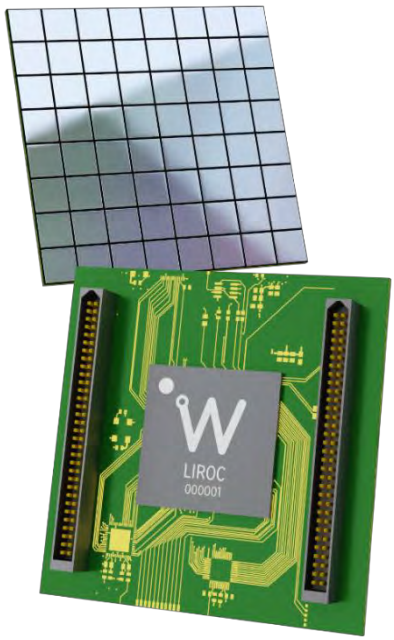
SiPM Analogue Read-out Chip for Lidar and Photon Counting Application

Liroc2 is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for LIDAR application.

Liroc2 allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 3 ns separated single photo-electrons). Liroc allows fast single photon counting over 300MHz per channel.

An adjustment of the SiPM high-voltage (gain) is possible using a channel-by-channel 6-bit DAC connected to the ASIC inputs. Channel-by-channel calibration on the trigger threshold is also possible thanks to 7-bit DACs. Liroc can be calibrated using the dark noise of the SiPM.

Liroc2 features a GHz measurement line composed of an RF preamplifier with pole zero cancellation followed by a fast discriminator and low swing LVDS fast driver.



Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 3ns double-peak separation on single photo-electron
Dynamic Range	Over 300MHz photon counting rate
Packaging & Dimension	BGA 20x20 mm^2 Flip-Chip low inductance packaging technology
Power Consumption	210mW – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 LVDS triggers
Internal Programmable Features (I^2C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7 bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp gain adjustment, individual trigger masking and cell powering.

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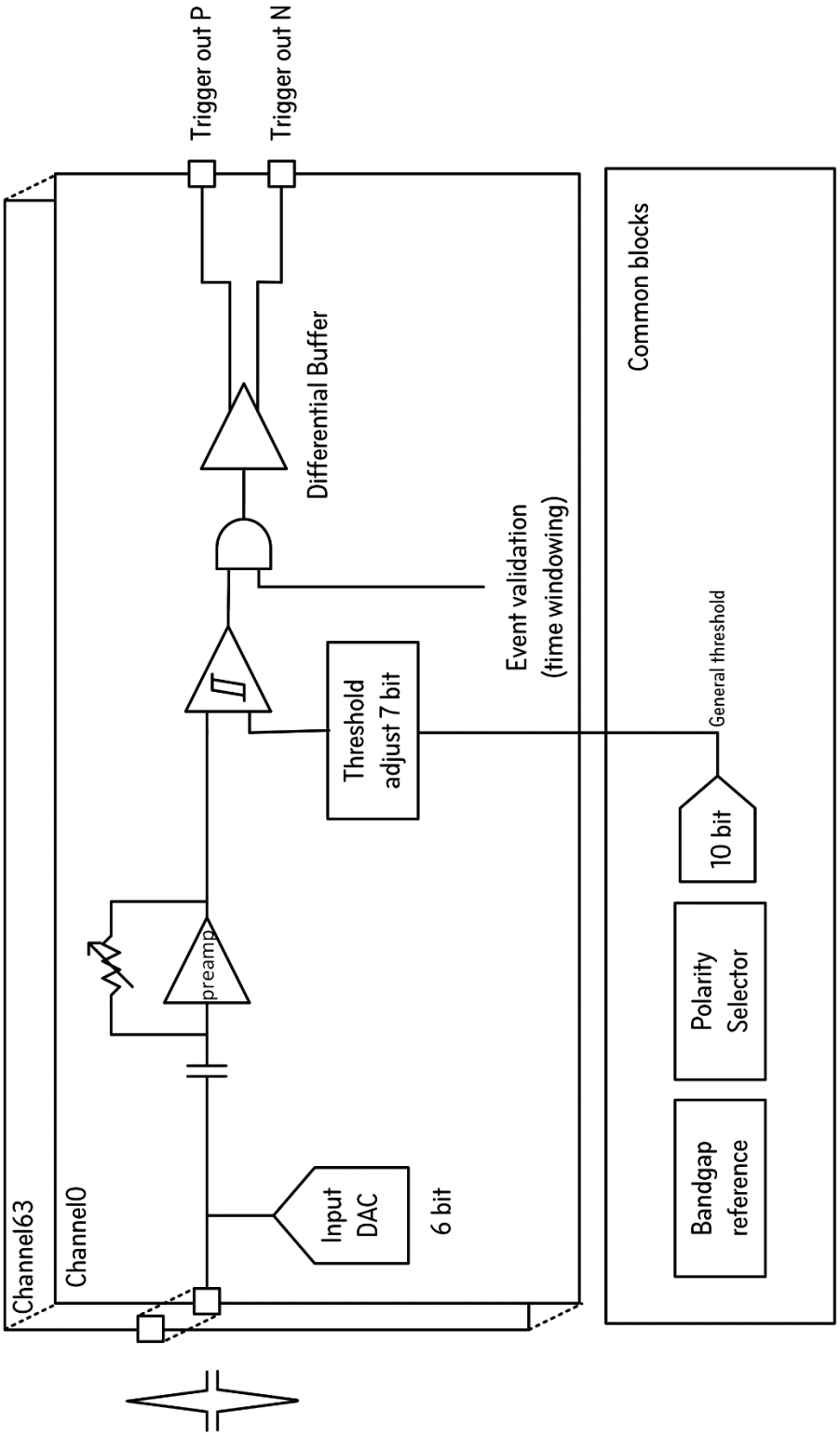
More about Liroc


Trigger out P
Trigger out N
Differential Buffer
Event validation
(time windowing)
Common blocks
General threshold
Threshold
adjust 7 bit
10 bit
Polarity
Selector
Bandgap
reference
preamp
Input
DAC
6 bit
Channel63
Channel0

weeroc

Temporoc

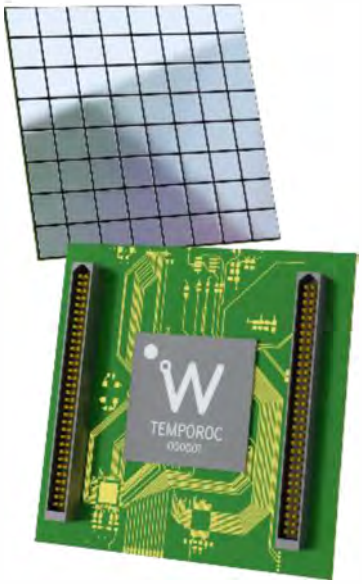
Multi-Purpose Mixed-Signal SiPM read-out ASIC

Temporoc is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) for particle time-of-flight measurement applications. Temporoc combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 40 ps-bin TDC. In total, Temporoc is capable of providing two distinct time tagging and two energy measurement of each event.

The concept of this ASIC is combining two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration. Additionally, Temporoc features clustering triggers readout which could be useful for particle detection with monolithic scintillator.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6.5 mW/channel. Temporoc is suitable for any application that requires both accurate time resolution and precise energy measurement such as time-of-flight gamma detection.



Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on first photo-electron
TDC precision	Below 50 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging & Dimension	BGA (20x20mm, 516 balls)
Power Consumption	410 mW (Power supply: 1.2V)
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (dual ADC and dual TDC per channel) – selectable transmission mode. 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), time trigger threshold adjustment (10bits), charge measurement tuning, ADC Peak Sensing, 64 trigger masks, internal temperature sensor, channel by channel output enable, trigger latch, programmable data output

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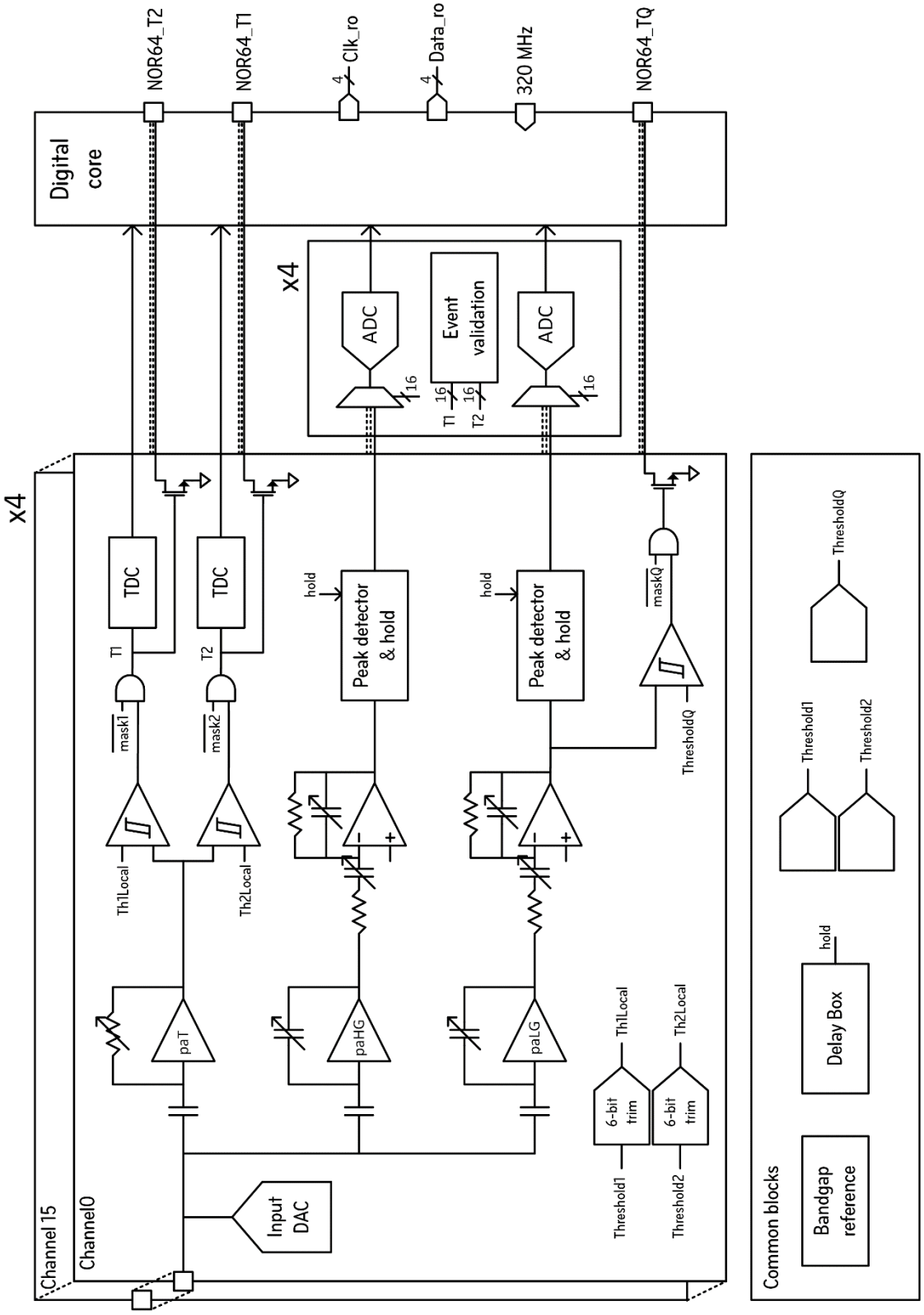
More about Temporoc


NOR64_T2
NOR64_T1
Clk_ro
Data_ro
320 MHz
NOR64_TQ
Digital core
x4
ADC
Event validation
ADC
16
T1
T2
x4
TDC
TDC
hold
Peak detector & hold
hold
Peak detector & hold
maskQ
ThresholdQ
T1
T2
mask1
mask2
Th1Local
Th2Local
paT
paHG
paLG
6-bit trim
6-bit trim
Th1Local
Th2Local
Threshold1
Threshold2
Input DAC
Channel 15
Channel0
Common blocks
ThresholdQ
Threshold1
Threshold2
hold
Delay Box
Bandgap reference

weeroc

Psiroc

PIN Diodes, Silicon Strips and GEMs Read-Out Chip

Psiroc is a 64-channel front-end ASIC designed to readout PIN diodes, silicon strips and GEMs, handling detector capacitances ranging from 0 up to few hundreds of pF.

Psiroc allows triggering down to 0.5 fC and provides dual-gain energy measurement with excellent Signal-to-Noise Ratio on the high gain (SNR over 10 for 0.5 fC) and large dynamic range on the low gain. For input signals over few pC a channel-wise ToT output is also available. Psiroc can be programmed to output the shapers HG/LG, individual triggers or ToT signals (two output pins per channels). The preamplifier gain is adjustable from 125 mV/pC up to 8 V/pC.

Charge measurement is done with peak detectors but those can be used in a track & hold fashion thanks to an internal delay cell. Analog data are outputted on two multiplexed analog output and can be read-out with an external ADC. Shapers shaping time can be adjusted from 20 ns to 3 µs with a step of 20 ns up to 300 ns and a step of 200 ns up to 3 µs.

Detector Read-Out	PIN Diodes, Silicon strips, GEMs
Number of Channels	64
Signal Polarity	Positive, negative
Sensitivity	Trigger on 0.5 fC on both polarity
Timing Resolution	< 150 ps RMS @ Q_{in} = 4 fC ; Cd/Cf = 20p/1p (pa gain = 1 V/pC)
Dynamic Range	Up to 5 pC with low gain charge measurement and up to 100 pC with ToT
Packaging & Dimension	BGA 20x20 mm^2
Power Consumption	350 mW – Supply voltage : 1.2 V
Inputs	64 analogue inputs
Outputs	2 outputs per channel, either : • 64 LVDS triggers • 2 x 64 TTL triggers • 64 TTL triggers and 64 analog outputs 2 multiplexed analogue outputs 3 NOR64 trigger outputs
Internal Programmable Features	3 trigger threshold tuning (10bits), channel-by-channel gain and shaping time adjustment (τ = 20 ns to 3 µs), individual trigger masking and cell powering.

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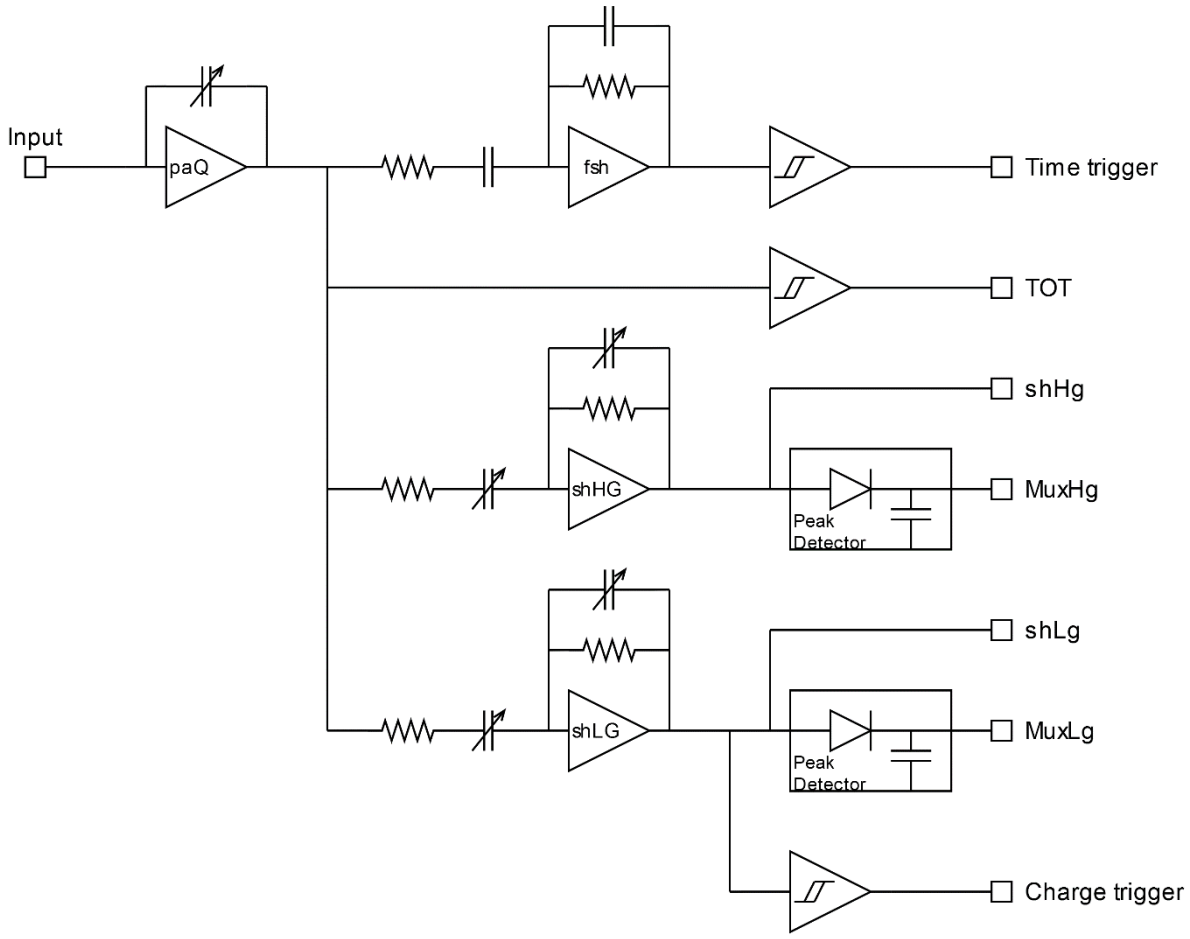
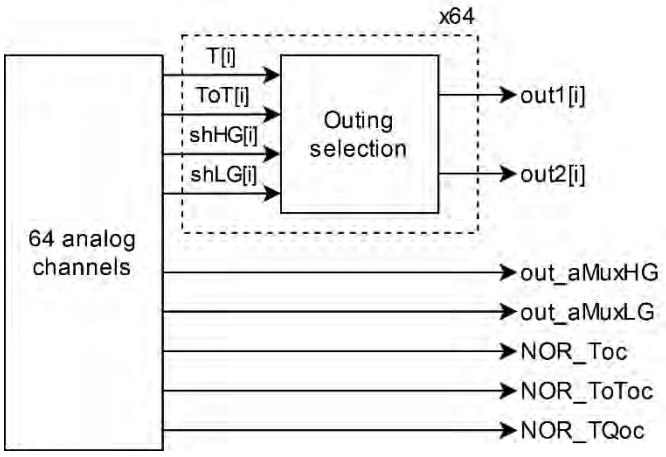
More about Psiroc



Simplified schematic of one channel. paQ – Charge preamplifier ; shHG – High Gain Shaper ; shLG – Low Gain shaper ; fsh – fast shaper



outing schematic

weeroc

Radioroc

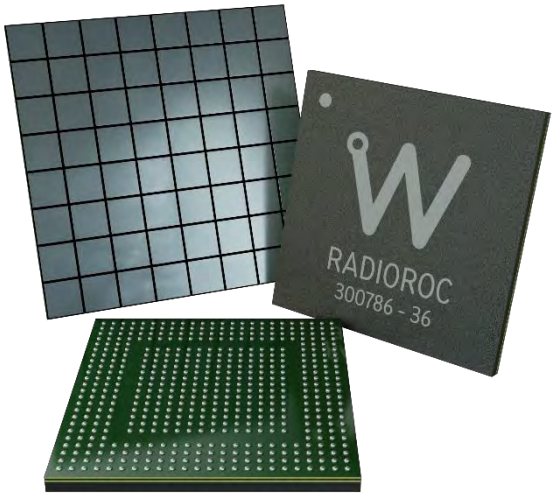
Dual Read-Out (Photon Counting & Charge Integration) Multi-Purpose SiPM Analogue Read-out Chip

Radioroc 2 is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM). Radioroc 2 allows triggering down to 1/3 p.e. and provides dual-gain energy measurement with excellent Signal-to-noise ratio on the high gain (SNR over 10 for single p.e.) and large dynamic range on the low gain.

Moreover, Radioroc 2 can output the 64-channel triggers with jitter as low as 55 ps FWHM on a single p.e. (160 fC, Cinj = 100pF). Photon-counting has been measured to be over 200 MHz. Time Over Threshold (TOT) can be used and has been measured to be able to handle the full input swing.

An adjustment of the SiPM high-voltage is possible using a channel-by-channel 8-bit DAC connected to the ASIC inputs to homogenize SiPM gains.

Timing resolution better than 55 ps FWHM is possible along with 1% linearity energy measurement up to 2000 p.e. Outputs can be selected via I^2C channel wise with 2 direct outputs per channel and the possibility to output single-ended/differential triggers or analog signals.



Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	55 ps FWHM on single photo-electron
Photon Counting	200 Mhz
Dynamic Range	Up to 2000 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	BGA 20x20 mm^2
Power Consumption	310mW – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	2 direct outputs per channel, selectable channel-per-channel, either: • 1 LVDS triggers • 2 TTL triggers • 1 TTL triggers and 1 analog outputs • 2 analog outputs 2 multiplexed analogue outputs and 3 NOR64 trigger outputs
Internal Programmable Features (I^2C)	64 HV adjustment for SiPM (64 x 8 bits), 3 trigger threshold tuning (10bits), channel-by-channel gain and shaping time adjustment (τ = 20 ns to 1800 ns), individual trigger masking and cell powering.

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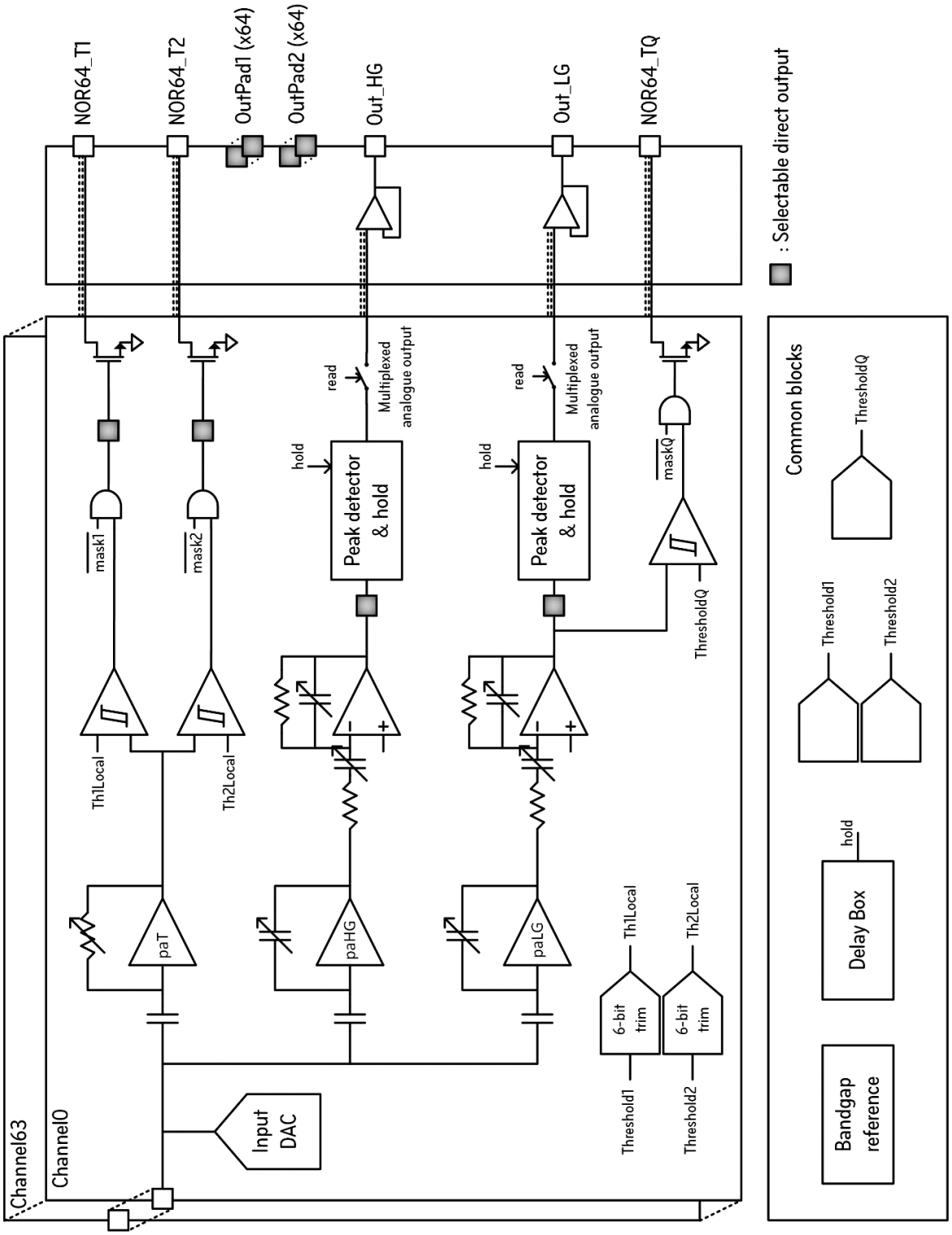
More about Radioroc

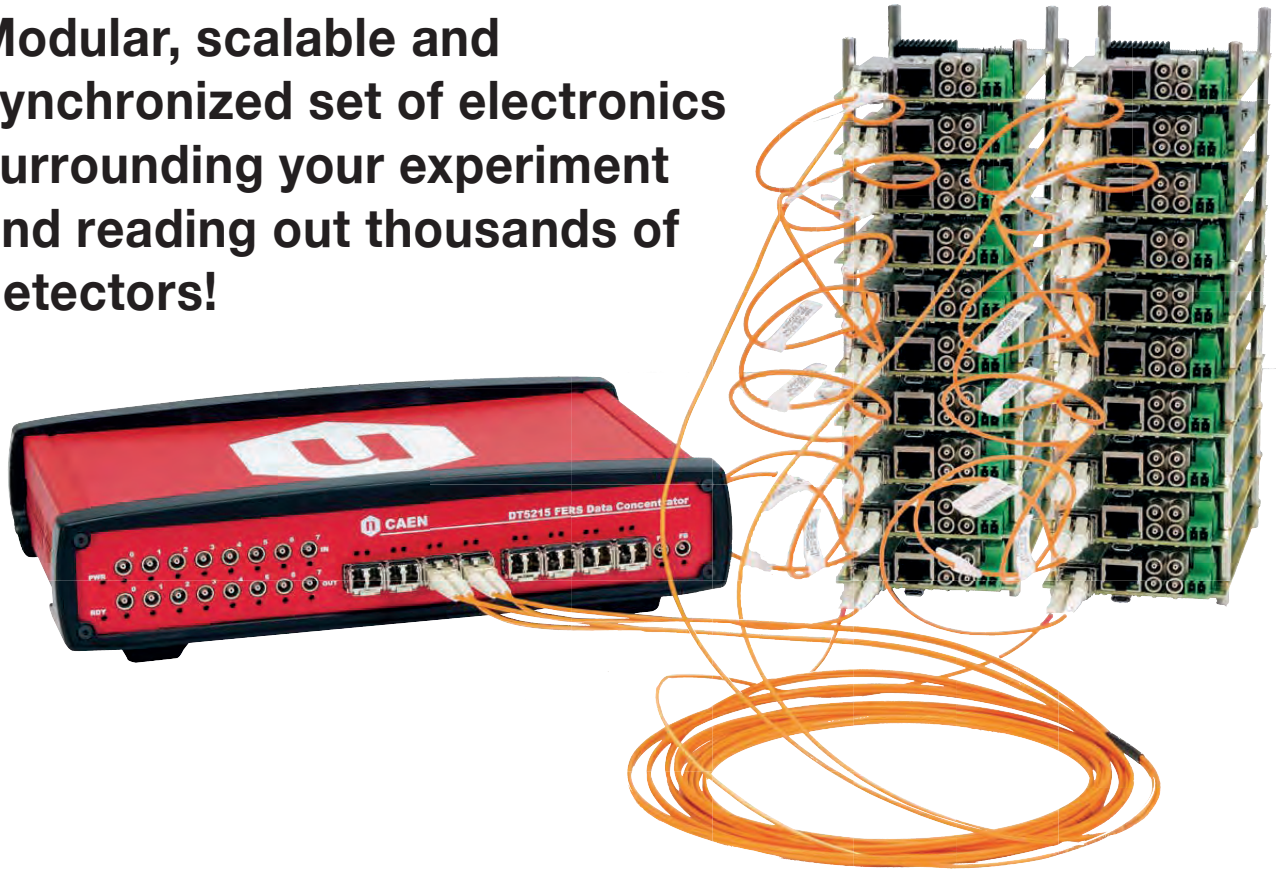


paT – Trigger preamplifier ; paHG – High Gain charge measurement preamplifier ; paLG – Low Gain charge measurement preamplifier.

FERS-5200 FAMILY

MODULAR FRONT-END READOUT SYSTEM

Modular, scalable and synchronized set of electronics surrounding your experiment and reading out thousands of detectors!



- **Modular front-end readout system based on high-density ASICs (CITIROC, picoTDC, RADIOROC, PSIROC, etc.)**
- **High channel count (64/128 ch per board) with low power and low cost per channel**
- **Scalable architecture: from standalone boards to synchronized networks with thousands of channels**
- **Optical daisy-chain synchronization via DT5215/DT5216* concentrators**
- **Managed via Janus software (customized per board type)**
- **Unified C++ control API with FERSlib for acquisition and slow control**
- **Ideal for SiPMs, PMTs, silicon strips, GEMs, wire chambers, and more**

*** COMING SOON**

HIGH CHANNEL DENSITY POWERED BY ASIC FRONT-ENDS

At the core of each FERS board is a carefully selected ASIC, chosen by CAEN to match the characteristics of specific detector technologies. Leveraging commercial chips such as CITIROC, picoTDC, and RADIOROC, FERS boards provide compact front-end solutions with 64 or 128 acquisition channels per module—optimizing both cost-per-channel and power efficiency.

The board-level design is the result of CAEN's long-standing collaboration with Nuclear Instruments, where electronics are engineered specifically around the chosen ASIC to ensure optimal analog performance and full digital integration. Starting with the A5204, FERS boards adopt a common PCB layout that ensures long-term compatibility with future Weeroc ASICs, thanks to their pin-to-pin equivalence. This strategy streamlines development while maintaining support for next-generation features without redesigning the entire system—ensuring continuity, scalability, and reliability.

A SCALABLE AND MODULAR READOUT ARCHITECTURE

FERS is designed to seamlessly scale from compact lab setups to large-scale experiments with thousands of channels. Each board integrates analog front-end, digitization or time stamping, acquisition logic, and communication interface into a compact, self-contained module. To offer maximum flexibility, FERS boards are available in two hardware configurations: the naked version, optimized for integration into mechanical frames and dense detector planes, and the desktop version, ideal for standalone use during prototyping, testing, or small-scale experiments.

Single-board systems can be powered and controlled directly via Ethernet/USB, while multi-board installations rely on a robust synchronization and data routing infrastructure based on optical TDlink connections and the use of DT5215 or DT5216 concentrators. These units ensure precise distribution of clock and control signals across the acquisition chain.

Importantly, the DT5215 also allows synchronization of the FERS system with external instrumentation, including CAEN digitizer families and GPS-based timing sources, enabling full integration into hybrid DAQ environments where precise time alignment is critical.

This architectural flexibility allows users to reuse the same FERS electronics across different scales and use cases, with minimal reconfiguration. Whether you're reading out a few SiPMs on the bench or managing timing for a large calorimeter array, FERS ensures consistency, precision, and ease of deployment—making it an ideal solution for both R&D environments and production-grade detector systems.

UNIFIED SOFTWARE CONTROL: JANUS & FERSLIB

FERS boards are controlled via Janus, CAEN's acquisition software tailored to each board type. Janus provides a graphical interface for configuration, monitoring, run control, and data visualization. Every board has its own version of Janus, optimized for its specific acquisition modes and parameters—whether you're working with pulse-height analysis, counting, TDC or streaming data. For advanced integration, the FERSlib C++ API allows users to develop custom acquisition and control applications. FERSlib abstracts hardware complexity, providing uniform access to registers, data buffers, and synchronization logic across the entire FERS ecosystem. Together, Janus and FERSlib streamline both development and operation, making the system accessible for users at all levels.

CONNECTIVITY & CONTROL HIGHLIGHTS

	10/100 Mb Ethernet	RJ-45 port on every FERS unit. Provides TCP/IP control and data at up to ~2–3 MB/s, ideal for standalone tests, firmware updates and fast prototyping. IP address, DHCP and basic health metrics are set in the on-board Web Interface.
	TDlink Optical Link	Optical link running proprietay TDlink protocol over duplex fiber (3.125 Gb/s) that combines clock, slow-control and data. One DT5215 hub fans out 8 links, each daisy-chaining up to 16 boards, for 128 units/ >8 k channels with <20 ps jitter and <6.4 ns fixed skew.
	USB 2.0	Micro-USB (front-ends) or USB-C (DT5215). Sustains ~ 3 MB/s and supports firmware upgrades or quick lab setups; synchronization is limited to single-board use.
	Embedded Web Interface	A browser-based GUI is available on all FERS boards. For single units, it allows network configuration and real-time status monitoring. On the DT5215 concentrator, it also provides TDlink control, log file download, and one-click FPGA/CPU firmware upgrade—no additional software required.
	USB 3.0, 1 GbE, 10 GbE	DT5215 equipped with USB 3.0, 1 Gb Ethernet, and 10 Gb Ethernet interfaces for data acquisition. USB 3.0 and 10 GbE support data rates up to ~300 MB/s, while 1 GbE offers ~100 MB/s—ideal for a wide range of system configurations.

A5202/DT5202

CITIROC-BASED 64 CH SIPM READOUT & BIAS

Flexible readout for single SiPMs or arrays. Full support for 64-channel matrices.

The A5202 (naked board) and DT5202 (desktop version) are compact, high-density front-end modules designed for the direct readout of Silicon Photomultipliers (SiPMs) within the CAEN FERS-5200 platform. Each unit integrates two Citiroc-1A ASICs, providing a total of 64 channels with complete analog signal conditioning and peak detection. Each channel includes a preamplifier, a fast shaper followed by a discriminator, and a slow shaper connected to a peak-and-hold circuit. The peak amplitude is acquired sequentially from each Citiroc-1A via a 13-bit external ADC under FPGA control, enabling accurate energy (pulse height) measurements. The fast shaper output is used to implement self-triggering per channel, as well as for Time over Threshold measurements, event counting, and the generation of a bunch trigger to start energy acquisition.

The module features a built-in A7585D programmable high-voltage supply to bias the connected SiPMs individually, eliminating the need for external HV sources.

The A5202/DT5202 can operate in standalone mode via USB or Ethernet for configuration and basic data acquisition. In larger systems, it connects via the TDlink protocol over optical fiber, which handles data readout, slow control, and synchronization to a DT5215 concentrator board. This allows multiple FERS units to operate in a fully synchronized and scalable acquisition system based on a common reference clock.

The system is fully supported by the Janus 5202 open-source software, which provides intuitive GUI and console-based control for configuration and data acquisition. For advanced integration, CAEN also provides the FERSlib C++ library, enabling users to develop custom applications and DAQ systems. A wide selection of input adapters, remote cabling options, and mechanical accessories is available to ensure compatibility with various SiPM formats and experimental setups. The A5202/DT5202 is an ideal solution for scalable, low-power front-end readout in applications such as particle and nuclear physics, medical imaging, and radiation monitoring.

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

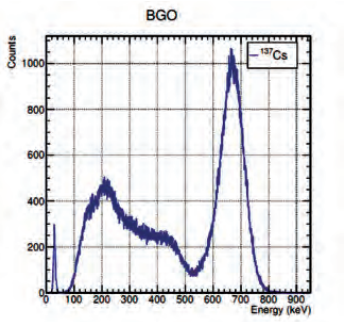
- Cosmic ray and particle detection
- Nuclear and gamma spectroscopy
- Calorimetry and high-energy physics
- Medical imaging and dosimetry

MORE INFO

A5202 DT5202

Amplitude Measurements with SiPM and ASIC (Citiroc 1A) Front-End Electronics.

Abstract - [...] In this paper, we describe a SiPM-based application with CAEN Front-End Readout System based on Citiroc 1A chip from Weeroc . Besides the use of this chip for well known single photon spectra and event counting, this paper exploits the possibility to acquire energy spectra directly from scintillators, paired with SiPM, through peak-and-hold readout. In particular, good energy resolutions have been achieved even with slow scintillators, like LYSO, CsI(Tl), and BGO, which have 40 ns, 1000 ns, and 300 ns of light decay time, respectively.[...] Several measurements have been performed using multiple radioactive γ sources and the resulting energy spectra demonstrate a resolution compatible with that found in literature [4] [5] [6] [7]. [...]



Calibrated energy spectra from 137Cs γ-radioactive source measured with BGO crystal coupled with single 6 × 6 mm2 SiPMs and acquired with the A5202 board.

See: Documentation Area - CAEN - Tools for Discovery/ AR9655 - Amplitude Measurements with SiPM and ASIC (Citiroc 1A) Front-End Electronics

A5203/DT5203

PICOTDC-BASED 64/128 CH HIGH-RESOLUTION TDC MODULE

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

- Particle tracking
- Time-of-flight (ToF) systems
- Fast detector R&D
- Synchronized multi-channel acquisition systems

MORE INFO

A5203 DT5203

The best achievable timing resolution in a compact form factor and optional dual-threshold discriminators.

The A5203 (and its desktop version DT5203) is a compact front-end module (~7 × 17 cm) within the CAEN FERS-5200 ecosystem, integrating the CERN picoTDC ASIC and providing 64 digital LVDS inputs (128 in the A5203B). Each channel timestamps rising and falling edges to reconstruct Time of Arrival (ToA), either as absolute time or as deltaT relative to a Tref pulse, and records Time over Threshold (ToT) for amplitude estimation and walk correction. At firmware level, a ToT filter rejects spurious low or saturated events, reducing noise and data throughput—especially valuable in high-rate environments.

Acquisition modes supported include Common Start, Common Stop, Trigger Matching, and continuous Streaming, allowing flexible operation in triggered or free-running scenarios

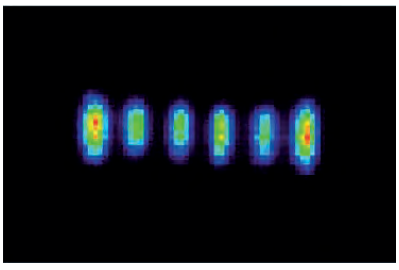
The TDC offers 3.125 ps LSB resolution with typical jitter around 7 ps RMS for fixed-amplitude signals, and about 20 ps RMS over a 50 dB dynamic range after walk correction via ToT .

Multiple A5203/DT5203 units can be synchronized using optical TDlink via the DT5215 concentrator (and the upcoming DT5216), enabling scalable multi-board systems with global timing alignment.

Full control and data acquisition is handled through Janus 5203, CAEN's open-source software suite for Windows and Linux, featuring both GUI and console modes for configuration, monitoring, run control, histogramming, and data export. For advanced users, the FERSlib C++ API enables development of fully customized acquisition and analysis software.

Picosecond timing measurements with the FERS-5200.

Abstract - [...] The A5203 FERS houses the recently released CERN picoTDC ASIC and provides high-resolution time measurements of Time of Arrival (ToA) and Time over Threshold (ToT). In this work we will analyze the performances of the A5203 unit: 3.125 ps LSB, ToA measurements down to ~7 ps RMS for signals of fixed amplitude over a single board, and ~20 ps RMS for input signals of variable amplitude (over a 50 dB dynamic range). The walk effect introduced by different amplitudes is corrected using the ToT. Besides walk correction, the ToT is used for signal amplitude reconstruction and background reduction. The A5203 has been used in various applications, both experimental and industrial. At the end of this work, its application in the ProVision PET scanner will be presented. Compactness, scalability and applicability to thousands of channels is required for the readout electronics.



Coronal view of a stack of 6 Na22 sources obtained during tests of the Picotech PET scanner.

See: https://pos.sissa.it/476/1203/

A5204/DT5204

RADIOROC-BASED 64 CH SIPM READOUT WITH HIGH-RESOLUTION TDC

Ideal for large SiPM arrays. Fully supports 64-channel matrices with bias and timing readout.

The A5204 (naked board) and DT5204 (desktop version) are advanced 64-channel front-end modules developed for high-performance readout of Silicon Photomultipliers (SiPMs) within the CAEN FERS-5200 ecosystem. At their core is the RADIOROC ASIC, specifically designed for fast and precise signal acquisition from SiPMs. Each channel includes a programmable preamplifier, dual-gain shaping chain, discriminator, and peak-and-hold logic, enabling both energy and time measurements. Timing is further enhanced by the integration of a 64-channel picoTDC ASIC from CERN, delivering sub-nanosecond resolution with 3.125 ps LSB.

The A5204 provides an internal programmable high-voltage generator (up to +85 V) and per-channel 8-bit DACs for fine SiPM bias adjustment, gain equalization, and temperature compensation. The fast discriminator line supports self-triggering down to 1/3 photoelectron, as well as majority and coincidence logic for trigger formation.

Data acquisition modes include spectroscopy, counting, and timing (common start/stop and streaming). Communication interfaces include USB, Ethernet, and optical TDlink, allowing the module to operate either standalone or as part of a synchronized multi-board system via the DT5215 or DT5216* concentrator.

Full control and data acquisition are provided by Janus 5204 open-source software, available in both GUI and console modes. For user-customized applications, the system is also supported by the FERSlib C++ API, enabling the development of tailored acquisition and control software.

* Coming soon

COMM. INTERFACES

10/100 M6E · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

- Precision timing and fast photon counting
- Dual-gain spectroscopy with SiPM detectors
- Scalable readout for large SiPM arrays
- Medical imaging and trigger-based acquisition

HIGHLIGHTS

- 64-channel front-end with RADIOROC + picoTDC architecture
- Dual-gain energy readout with programmable shaping for PSD
- Sub-nanosecond timing resolution (55 ps FWHM, 3.125 ps LSB)
- Internal HV generator up to +85 V with per-channel DAC trimming
- Fast self-triggering down to 1/3 photoelectron
- Multiple acquisition modes: spectroscopy, timing, counting
- Full support for trigger logic, coincidences, and majority logic
- Standalone or scalable setup with TDlink optical daisy chain
- Real-time control and visualization with Janus 5204 software (GUI/Console)
- Compact size, USB/Ethernet/TDlink interfaces, low power consumption
- For user-customized applications, the system is also supported by the FERSlib C++ API, enabling the development of tailored acquisition and control software.

MORE INFO

A5204 DT5204

COMING SOON

A5205/DT5205

PSIROC-BASED 64 CH CHARGE & TDC READOUT MODULE

Ideal for precision readout of silicon strips, GEMs, and PIN diodes in high-resolution tracking and low-charge detection systems.

The A5205 (board version) and DT5205 (desktop version) are 64-channel front-end modules of the CAEN FERS-5200 family, designed for the high-resolution readout of PIN diodes, silicon strip detectors, and GEMs. At their core is the Weeroc Psiroc ASIC, coupled with the CERN picoTDC chip, enabling precise charge and timing measurements for capacitive detectors operating at very low signal levels.

Each channel features a charge-sensitive preamplifier with programmable gain from 125 mV/pC up to 4 V/pC, followed by a shaping stage and peak detector. The input stage accepts both positive and negative polarity signals. Psiroc enables triggering down to 0.5 fC on sub-20 pF detectors, and supports dual-gain charge measurement. For input charges above a few pC, a channel-wise Time over Threshold (ToT) output is also available, providing high-rate, low-dead-time pulse amplitude estimation without the need for multiplexed ADC conversion.

Data acquisition can operate in global or per-channel mode, with individual triggers routed to the integrated picoTDC, offering sub-nanosecond timing resolution (3.125 ps LSB). Timestamp and PHA acquisition are fully supported.

The A5205/DT5205 includes synchronization and communication interfaces (USB, Ethernet, and TDlink) and is fully managed by the Janus 5205 open-source software, available for Windows® and Linux®. A complete set of dedicated accessories—cables, adapters, and remote connectors—is available to support a wide range of detector formats and experimental configurations.

COMM. INTERFACES

10/100 MbE · USB 2.0 · TDLINK

SOFTWARE & LIBRARY

WEB INTERFACE · JANUS FERS CAEN · CAEN FERSlib

APPLICATIONS

- Silicon strip and pixel detectors
- Micro-pattern gaseous detectors (GEM, Micromegas)
- PIN diode arrays for beam and dose monitoring
- High-precision tracking and timing in nuclear physics

MORE INFO

A5205 DT5205

HIGHLIGHTS

- 64-channel readout with Weeroc Psiroc ASIC
- Triggering down to 0.5 fC for sub-20 pF detectors
- Dual-gain charge measurement and ToT output
- Sub-ns timing resolution with picoTDC (3.125 ps LSB)
- Positive/negative input polarity supported
- Adjustable gain up to 4 V/pC, shaping from 20 ns to 3 µs
- Low dead time acquisition without multiplexed ADC
- Fully supported by Janus 5205 software suite

DT5215

CONCENTRATOR BOARD FOR FERS-5200

The DT5215 Concentrator Board manages synchronization and data aggregation from multiple FERS units within the CAEN acquisition ecosystem. It provides 8 optical links running the CAEN TDlink proprietary protocol, each capable of daisy-chaining up to 16 FERS boards, for a total of up to 128 modules per concentrator—corresponding to several thousand acquisition channels, depending on the configuration.

At the heart of the concentrator is an embedded Linux-based single board computer, which supervises the FERS network and collects data fragments from each unit. These fragments are transmitted directly to the host computer through high-speed communication interfaces, including USB 3.0, 1 Gb Ethernet, and 10 Gb Ethernet, supporting data rates up to 300 MB/s.

Multiple DT5215 boards can be synchronized to build scalable, distributed acquisition systems with unified timing. Synchronization can also be extended to CAEN digitizer families, enabling time-correlated acquisition across heterogeneous systems. In such cases, FERS modules and digitizers typically run under separate acquisition software, unless the user develops a custom unified solution using the available software libraries.

The DT5215 is fully supported by CAEN's Janus software for system configuration, monitoring, and control, and by the FERSlib C++ API, which allows users to develop custom acquisition and data handling applications.

COMM. INTERFACES

USB 3.0 | 1 GbE | 10 GbE

FEATURES

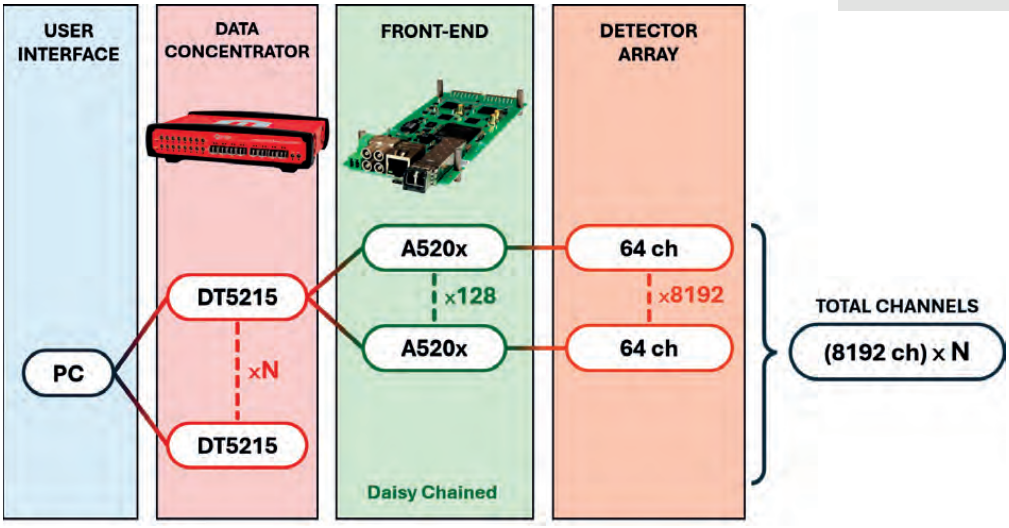
MULTI BOARD SYNC

SOFTWARE & LIBRARY

WEB INTERFACE | JANUS FERS CAEN | CAEN FERSlib

HIGHLIGHTS

- Concentrator board for multiboard management in FERS-5200, the CAEN platform for the readout of large arrays of detectors (SiPM, MA-PMTs, Gas Tubes, Si detectors, ...).
- Scalability: from a single standalone FERS unit for prototyping to many thousands of channels, with simple tree network structure.
- Modularity: multiple FERS units can be distributed on large detector volume and managed by a single Concentrator board.
- 8x TDlink for event data building, processing and formatting.
- Easy-synch: one single optical link (TDlink) for data readout, slow control and boards synchronization.
- Available also in single TDlink version (DT5216): supports up to 8 FERS units in daisy chain.



NOTE: using the A5203B the channel numbers are doubled

MORE INFO

COMING SOON

DT5216

COMPACT DATA CONCENTRATOR FOR FERS-5200S

Ideal for mid-scale detector setups. Manages up to 8 FERS units with synchronized readout and control.

The DT5216 is a compact Data Concentrator developed for the CAEN FERS-5200 platform, designed to manage small-to-medium scale readout systems based on front-end units such as the A5202, A5203, A5204 and A5205. It features a single TDlink optical port and supports up to 8 FERS units in daisy chain, allowing the acquisition of up to 512 channels when used with 64-channel front-end boards. TDlink handles data transfer, slow control, and timing synchronization over a single optical connection, significantly simplifying system architecture.

Communication with the host PC is provided via high-speed USB 3.0 (Type-C), ensuring fast data throughput and streamlined setup. The DT5216 is ideal for prototyping, beamline tests, and mid-scale experiments requiring synchronized, multi-board operation without the complexity of a full-scale system. Its compact size and low channel count make it a cost-effective alternative to the DT5215 concentrator, while maintaining compatibility with the entire FERS-5200 ecosystem.

Firmware is upgradable via USB, and synchronization performance is optimized through software compensation of optical delays, achieving typical clock jitter of 20 ps and fixed skew under 6.4 ns. The DT5216 offers a scalable path to future system expansion, providing the same user interface and DAQ software tools as larger FERS deployments.

COMM. INTERFACES

USB 3.0

SOFTWARE & LIBRARY

JANUS FERS CAEN

CAEN FERSlib

HIGHLIGHTS

- Compact concentrator for up to 8 FERS units via TDlink
- USB 3.0 host interface with up to 300 MB/s readout rate
- Full synchronization: data, control, and timing over one link
- Ideal for prototyping and distributed DAQ setups
- Firmware upgradeable via USB; plug-and-play operation
- Seamless integration with Janus software and DT5215-based networks

MORE INFO

NOTE: using the A5203B the channel numbers are doubled

JANUS

FERS-5200 DAQ SOFTWARE

A single DAQ software to control the FERS-5200 board family. Available in Console and GUI Mode, it allows the user to customize the DAQ, and offers an easy way to approach multi-boards and high-channel density FERS-5200 systems.

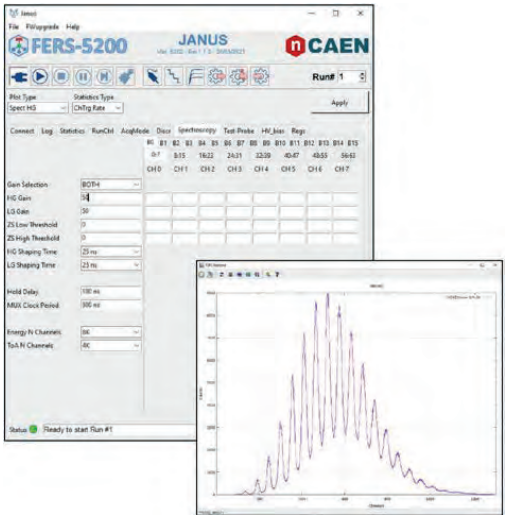
Janus is an open source software for the control and readout of FERS-5200 boards. Available in two versions (Ver. 5202, Ver. 5203), it can be used as a platform for the development of custom DAQ, tailored to the specific application. Indeed, the user can change the data treatment, the acquired statistics and the output file format.

Janus can manage up to 16 FERS units connected via Ethernet or USB directly as well as the readout of the DT5215 Concentrator Board, so that a single user interface is available for the whole system.

Janus is composed of two parts, one written in C, which is the real heart of the application, one written in Python which manages the user interface. The plots are executed through Gnuplot. All the configuration parameters are written in a textual configuration file.

It is possible to launch and use Janus in 2 different modes:

- **Console Mode**. In this case, the Python part of the software is not used. The user can edit the configuration file with any text editor and save the proper values for the desired parameters. Then, the user can launch a purely textual console window. The application writes a series of messages (which are also saved in a log file) and, during the run, prints statistics on the screen. The only graphical part is the plot, which is managed by Gnuplot.
- **GUI Mode**. In this case, the user only have to run the Python program which calls the C program and connects to it via a socket to send commands and receive messages which are then displayed in the Python GUI.



HIGHLIGHTS

- Model-dependent GUI for a quick and easy start
- Open-Source for user customization
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in .bin, .txt format
- Statistics and Plots visualization

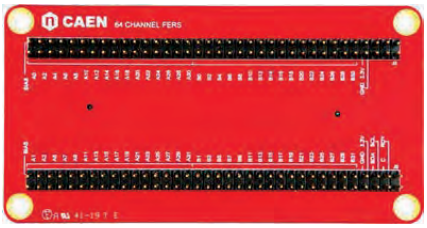
MORE INFO

MORE INFO

ACCESSORIES
FOR FERS-5200

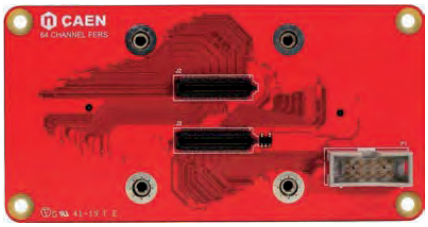
A5250

Converts 2.54 mm pitch pin headers to FERS-5200 input format, enabling direct connection of SiPMs or similar detectors to CAEN A5202 and A5204 front-end readout boards.



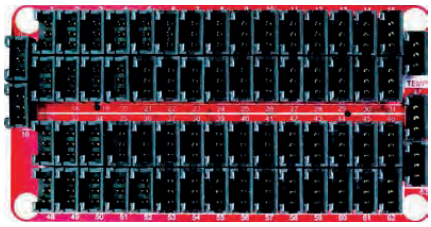
A5251

Interfaces Hamamatsu S13361-3050AE-08 SiPM matrices with A5202 and A5204 boards, providing direct signal routing to FERS-5200 inputs via Samtec-compatible high-density connectors.



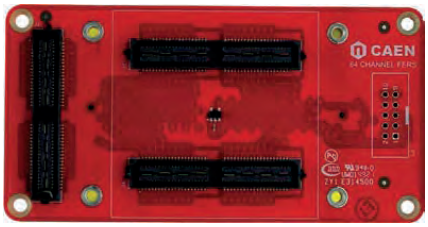
A5253

Ideal for connecting individual SiPMs to A5202 and A5204 boards via 3-pin connectors; compatible with A5261 cable for low-noise, remote signal transmission to FERS-5200 inputs.



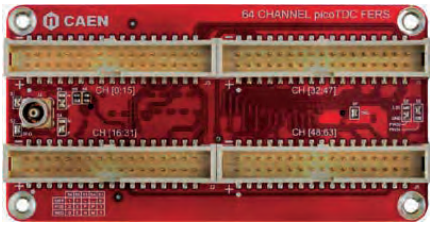
A5254

Connects OnSemi SiPM matrices (ARRAYJ/ARRAYC-60035-64P-PCB) to A5202 and A5204 boards using high-density Samtec connectors, ensuring reliable signal transfer to FERS-5200 inputs.



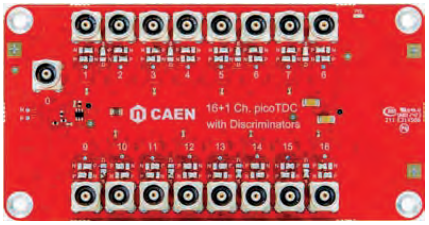
A5255

Provides direct connection of 64 LVDS differential inputs to A5203 via 2.54 mm pitch quad-row header, allowing signal routing from custom detectors to the FERS-5200 TDC system.



A5256

Provides 16+1 single-threshold or 8+1 dual-threshold edge discriminators for single-ended signals, delivering LVDS outputs to A5203 for time digitization in FERS-5200 systems.



A5260

Flat cable with 2.54 mm pitch connectors, used to place FERS boards away from front-end adapters, reducing mechanical constraints near the detector.

A5261

Shielded cable with 3-pin connectors designed to route single-ended signals to A5202/A5204 inputs via A5253 adapter, ensuring low-noise remote connection.

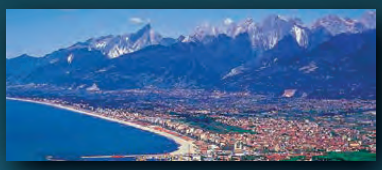
A5270

Fan unit for FERS boards, used when ventilation is limited or when required by system specifications to ensure proper cooling of non-boxed modules.

CAEN global presence

CAEN Worldwide presence CAEN SyS

CAEN Technologies, Inc.
Staten Island, NY • USA



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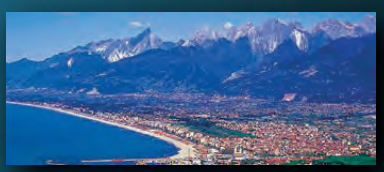

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