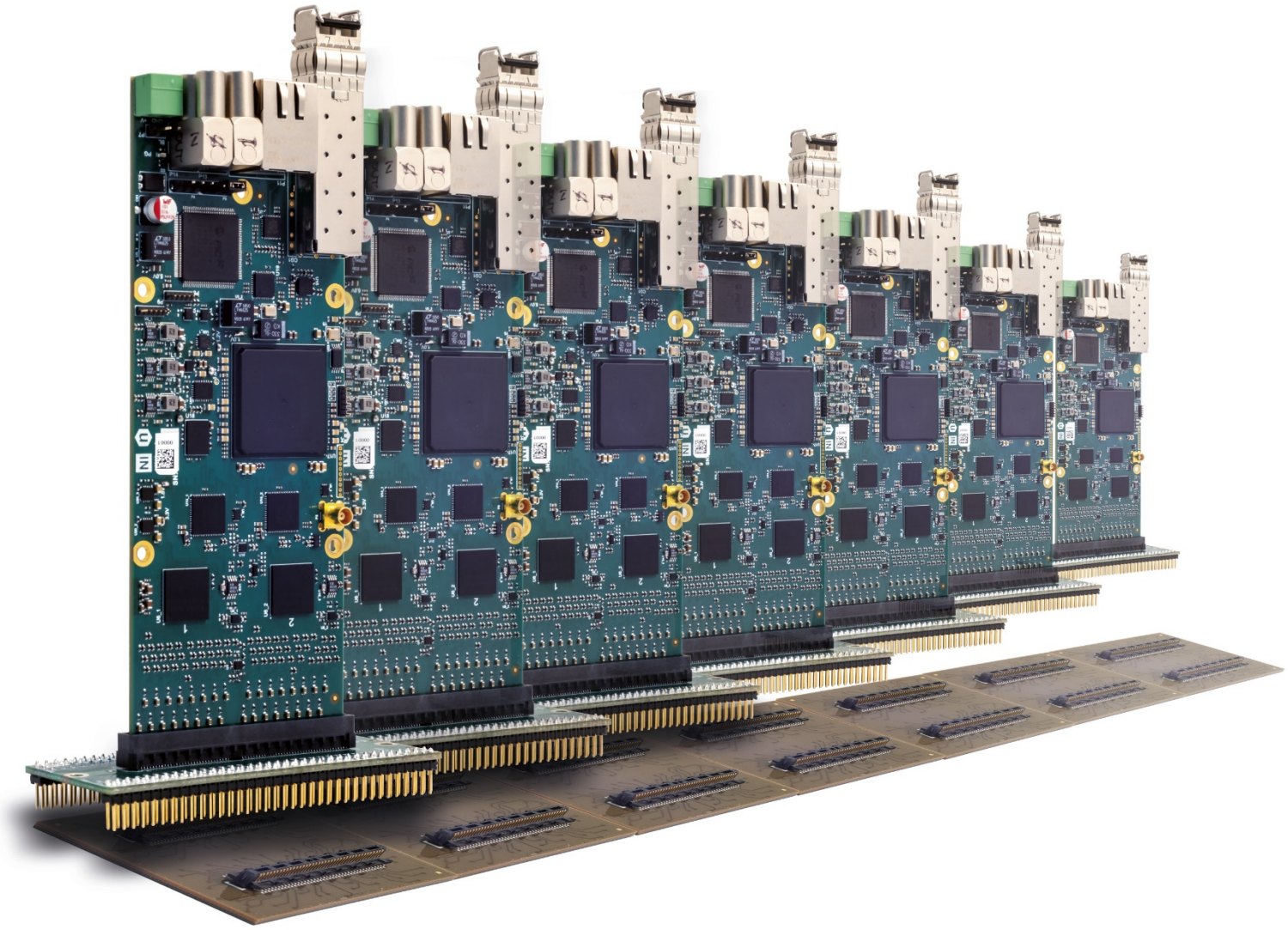

FERS-5200

Front-End Readout System

Datasheet

DS7218

CAEN SpA
Via Vetraia 11
55049 – Viareggio Italy
Tel +39.0584.388.398
Fax +39.0584.388.959
info@caen.it www.caen.it

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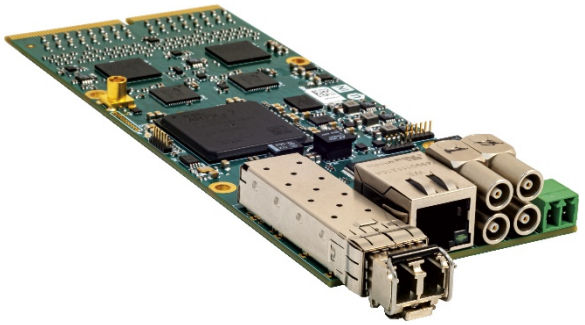
FERS-5200

Front-End Readout System

Modular, Scalable, Cost-effective:
all you need for your system is in FERS-5200

Particle Physics *Medical Applications* *Nuclear Physics*



HIGHLIGHTS

- Platform for the **readout of large arrays of detectors** (SiPM, MA-PMTs, Gas Tubes, Si detectors, …)
- **Versatility:** a **family of Front-End cards** (FERS units) tailored for different detectors.
- **Scalability**: from a single standalone FERS unit for prototyping to many thousands of channels, with simple **tree network** structure.
- **Modularity**: multiple FERS units can be distributed on large detector volume and managed by a single Concentrator board.
- **Flexibility**: possibility to fit different front-end in the same architecture.
- **Compactness**: front-end cards with high channel density ASICs and effective connection to the detector backplane
- **Easy-synch**: one single optical link (TDlink) for data readout, slow control and boards synchronization.
- **Acquisition modes**: spectroscopy (PHA), counting, time stamping, waveform recording, depending on the Front-End ASIC
- **Concentrator Board** with multiple TDlink for event data building, processing and formatting.
- **Boxed FERS unit** for desktop use or naked for customizable mechanical frames.

OVERVIEW

FERS-5200 is a Front-End Readout System designed for the readout of large detector arrays, such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEM, Gas Tubes and others.

FERS is a **distributed** and **easy-scalable** platform, where each unit is a small card that houses 32 or 64 channels with Front End electronics, A/D converters, trigger logic, synchronization, local memory and readout interface.
FERS is a **flexible platform**: keeping the same readout and control infrastructure, that is the same user interface, different types of front-end can be developed to fit a variety of detectors. In most cases, the front-end is based on ASIC chips that allow for high density, cost-effective integration of multi-channel readout electronics into small size and low power modules. The Front End ASIC can implement an analog chain made of preamplifier, shaper, peak sensing and discriminator: this is the case of the model **A5202,** based on the Citiroc-1A chip produced by Weeroc for SiPM readout. In other cases, the ASIC is a fast flash ADC (1 GS/s or more) that records the waveform of the input pulses and makes it possible to apply digital algorithms providing timing, energy and pulse shape information.

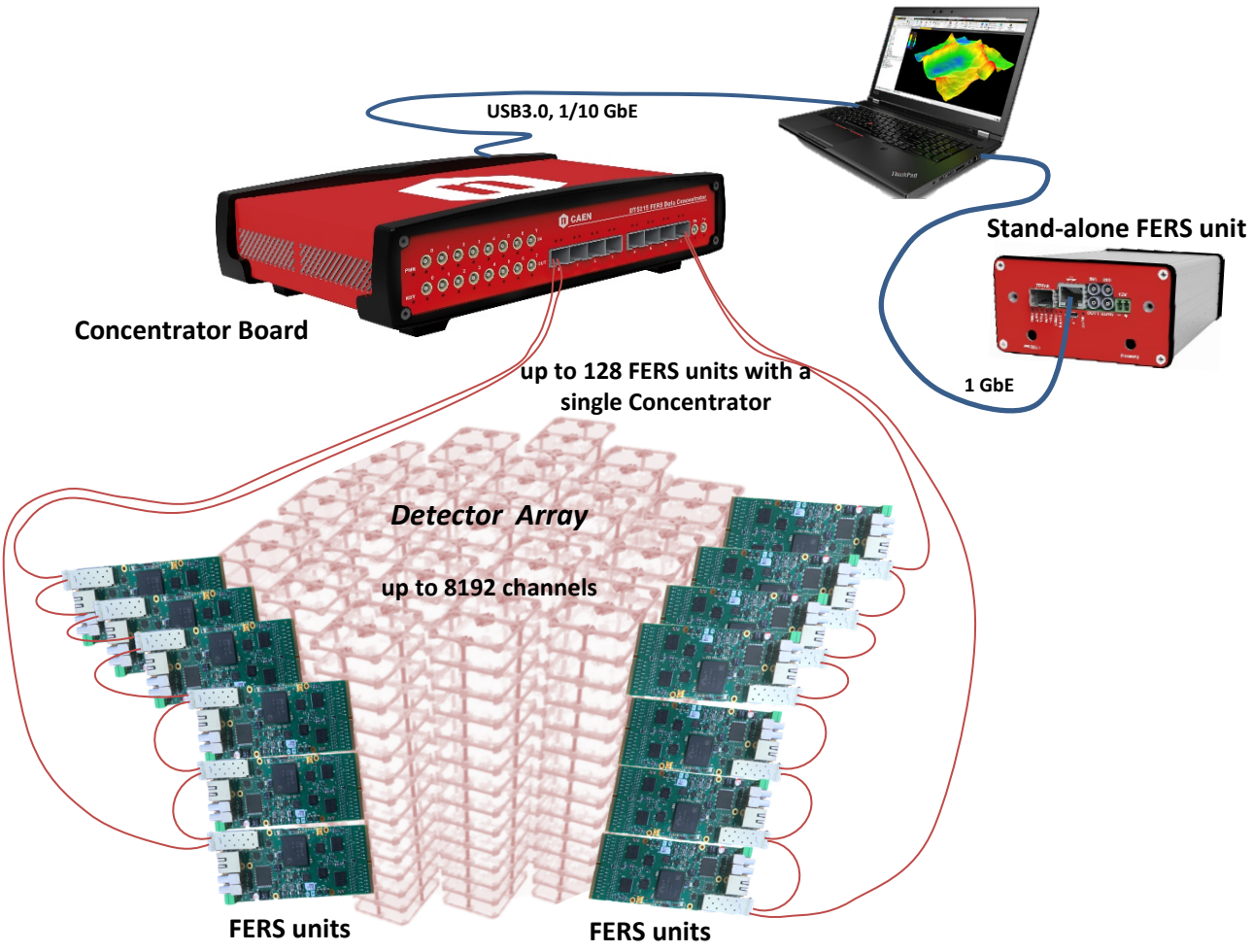
One FERS unit can be used **stand alone**, without any additional hardware, just connected to the computer via USB 2.0 or Ethernet 10/100T. This is a cheap and an easy-to-use evaluation board of the specific ASIC chip housed on the FERS unit. Once the solution is validated, scaling up to thousands channels is immediate: multiple FERS units can be connected in a **tree network**, where the optical **TDlink** is the unique physical connection that guarantees high throughput data readout, slow control and accurate timing synchronization.

One **DT5215 (FERS Data Concentrator)** can manage up to 8 TDlinks, each connected to 16 FERS units in daisy chain: in the case of the A5202 (CITIROC 1A), it makes 8192 readout channels. The Data Concentrator is connected to the Host computer through 1/10 Gb Ethernet or USB 3.0. Multiple concentrator boards can be synchronized in order to further extend the total number of channels.
A Linux-based Single Board Computer is embedded in the Concentrator board. It manages the data readout from the network of FERS units and the event data building according to the time stamp and/or trigger ID of the event fragments acquired by each unit. Sorted and merged data packets are then stored to the local memory and finally sent to the host computers through a fast 10 GbE or USB 3.0 link. Custom algorithms for data processing and reduction can be easily uploaded by the user into the embedded CPU.

DT5215 Concentrator Board (left) and A5202 boxed for desktop use (right)

FERS-5200 at work!

The tree network for large systems building



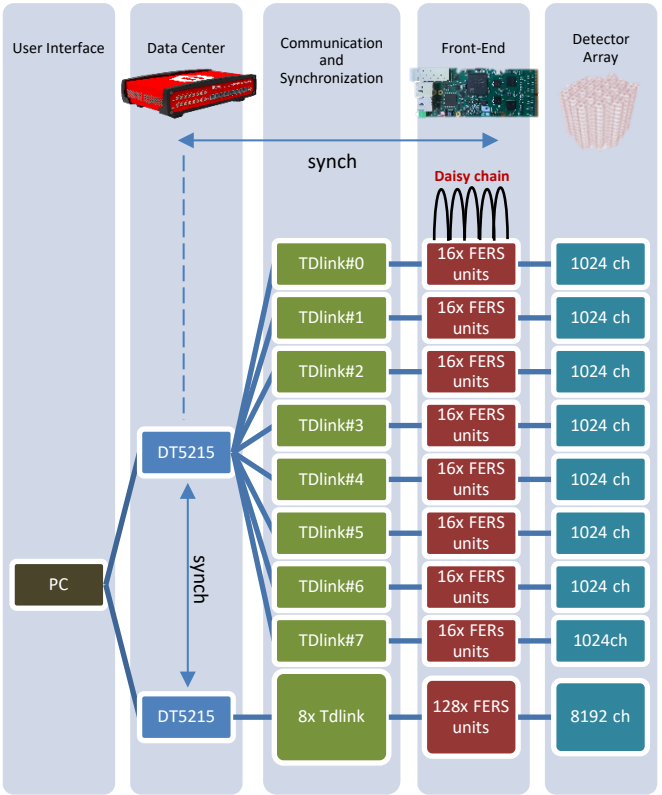
One computer, one Concentrator, thousands of channels

FERS-5200 is an extendable system: the same FERS unit can be used either as stand-alone or as part of the network tree for the readout of large arrays of detectors. In this way, the same card and same interface will be used, starting from the prototyping phase till the final implementation of the experiment.

The core of the scalability of the FERS-5200 is the optical **TDlink**, which manages data stream, slow control and synchronization at once.

The concentrator board DT5215 hosts 8 optical links, each one sustaining up to 16 FERS units in daisy chain. In the case of A5202 for SiPM readout, this means **8192** channels managed by a single Concentrator board.

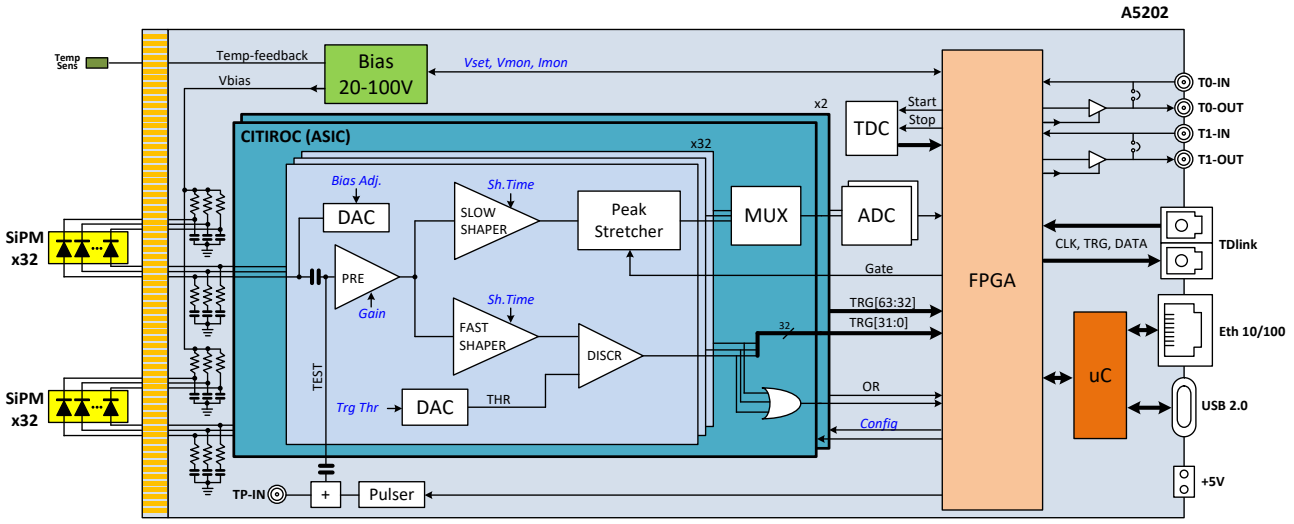
Further scalability is possible if synchronizing **more than one Concentrator board**.



The first member of the family: A5202

Equipped with CITIROC 1A ASICs for **SiPM** readout

The **A5202** is a small board (~ 6 x 15 cm) housing two CITIROC ASIC chips (64 channels in total), the ADCs, the FPGA, the bias power supply for the SiPMs and the interfaces for readout, synchronization and control.



Simplified block diagram of the FERS unit A5202 with CITIROC ASICs

Technical Specifications (PRELIMINARY)

Number of Inputs	64 (= 2 CITIROC 1A chips)
Signal Polarity	Positive
Sensitivity	Low Gain = 1.5pF/Cf (max gain = 60). High Gain = 15pf/Cf (max gain = 600)
Dynamic Range	Max: 400 pC (i.e. 2500 photo-electrons @ 10^6 SiPM gain)
Shaping Time	7 options from 12.5 to 87.5 ns
Self-Triggers	Min threshold = 1/3 photo-electron. Separate trigger lines per channel
External Trigger	From TDlink or T1 input.
Bias Voltage	Common bias: 20 to 100V. Individual adjust: 8 bit, 4.5V range
Counting mode	Max. 20 Mcps, independent channels, 32 bit depth
Spectroscopy Mode	Simultaneous acquisition. 13 bit A/D conversion. Max conversion time = 10 µs
Timing Mode	0.5 ns resolution. Independent channels (merged list, time sorted) Spectroscopy information (low res) from ToT (0.5 ns). Linearization LUT.
Trigger Time Stamp	48 bit, 2.5 ns step (~195 hours)
Zero/Ovr Suppression	Independent digital thresholds (LLD, ULD) and/or self-trigger mask
Readout/Control Interface	TDlink (6.25 Gbit/s) optical link with synch distribution. Ethernet 10/100T. USB 2.0
Power Requirements	Single power supply (+12V). Max current t.b.d.
Size	Approx. 60 x 150 x 20 mm

Ordering Option

Ordering code	**Description**
WA5202XAAAAA	A5202 – 64 channel CITIROC unit for FERS-5200
WDT5215XAAAA	DT5215 – Collector board for FERS-5200

CAEN SpA
Via Vetraia 11
55049 – Viareggio Italy
Tel +39.0584.388.398
Fax +39.0584.388.959
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