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High-end Microelectronics Design

Read-Out Chips Catalog

Small details
Great differences

CAEN
Tools for Discovery

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CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

CAEN GmbH

Klingenstraß e 108
42651 - Solingen • Germany
Phone +49.212.2544077
Fax +49.212.2544079
info@caen-de.com
www.caen-de.comt

CAEN Technologies, Inc.

1140 Bay Street - Suite 2C
Staten Island, NY 10305 • USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

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High-end Microelectronics Design

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CAEN is the exclusive Weeroc Worldwide distributor, providing ASICs and ASICs-based development systems for the industry and the physics community.

WHAT WE DO

ASICs

Weeroc designs and provides analog and mixed ASICs for science and industry

Testboard

The simplest way to work with Weeroc ASICs

DT5550W

CAEN development and DAQ platform with programmable FPGA designed to read out multiple Weeroc ASICs

DT5702
APPLICATION

CAEN solution based on Weeroc CITIROC ASIC for the readout of SiPM arrays (p. 28)

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High-end Microelectronics Design

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CAEN and Weeroc

Weeroc is a spin-off company from Omega laboratory (IN2P3/CNRS French governmental agency for fundamental research in astrophysics, particle physics and nuclear physics) and today offers a full range of products to read out almost any kind of detector. In particular, it provides off-the-shelf programmable analog and mixed front-end ASICs for photon and particle detectors readout, together with Testboards specifically designed for each ASIC.

Weeroc main customers are the major actors in the fields of:

- Medical imaging
- Homeland security
- Nuclear protection
- Scientific instrumentation
- Space (launchers and satellites)

In order to widen the adoption of Weeroc ASICs, CAEN developed specifically the DT5550W a system designed to extensively test the ASICs. The DT5550W has a user programmable FPGA allowing the user to characterize the performance of one or multiple chips and build a complete DAQ system.

Moreover CAEN offers a solution (DT5702 see p. 28) based on CITIROC ASIC, for SiPM arrays readout.

Weeroc designs high-performance analog and mixed signal ASICs

We know there is a long way from a good idea to a good product. Weeroc provides all services to get your innovative project up and running. We are committed to fast and efficient design that will allow your product to embed dedicated state-of-the-art microelectronics in no time.

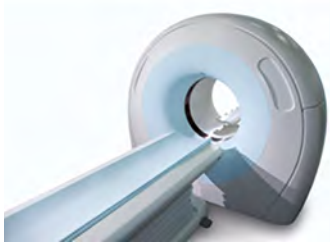
We can handle your project from the specification definition to the production and integration of your ASIC in your system.

Photodetectors read-out

What is the point to have state-of-the art photodetectors if you loose half the perfs in the first stage of your readout electronics?

Weeroc designs fully-integrated, low-power front-end ASICs. We can get the best out of your photodetectors.

Weeroc team has altogether over a century of experience in photodetector readout. When it comes to photodection, we know what we are talking about.



State-of-the-Art Medical Imaging

Anyone in the medical imaging field knows there is a major trend for number-of-channel increase in the upcoming systems. Furthermore, future medical imaging equipments will feature multi-modality and extreme sensitivity for better diagnostics and faster acquisition.

More channels, less room, less power budget, better performance... Weeroc designs customer specific readout chips to help them achieve the upcoming technical breakthrough in the medical imaging field.

Radiation Tolerant Design

Weeroc team comes from high energy physics field. They have designed rad-hard ASICs that are currently installed in CERN and in other worldwide research facilities.

Specific requirements such as radiation hardness, large temperature range, failure analysis is something we are used to.

Summary

Weeroc offer a full range of product to read-out almost any kind of detectors. The table below describes which read-out chip is suitable for which kind of detectors. Weeroc application engineers can help you choose the best fit for your detector and application.

	SiPM	MA-PMT	PMT	APD	Pin diode	Silicon strips	RPCs	Micromegas GEMS
Maroc 3A	×	✓	✓					
Catiroc 1	✘	×	✓					
Spaciroc 3	×	✓	✓					
Citiroc 1A	✓							
Petiroc 2A	✓						×[1]	
COMING SOON Photoroc 1A	×	✓	✓					
Triroc 1A	✓							
Skiroc 2A				✓	✓	✓		
Hardroc 3B	×	×					✓	
Gemroc 1				✘	✘	✘		✓

✓ Optimized for - × Compatibility - ✘ Compatibility (not tested)

[1] Petiroc can read RPCs on the trigger line solely, no compatibility on the energy measurement line

Weeroc products maturity is ranged using the TRL scale. The Weeroc definition of TRL is described below.

Technology Readiness Level	Description
TRL 1	ASIC project
TRL 2	ASIC in foundry
TRL 3	silicon available
TRL 4	First measurements, bug detected
TRL 5	First measurement, conclusive in lab
TRL 6	Application prototype available
TRL 7	Full system using ASIC available
TRL 8	Full system using ASIC running
TRL 9	Full system running ASIC , relability proven

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Summary

Weeroc read-out chips main features and specifications are summarized in the table below.

	Maroc	Hardroc	Gemroc	Skiroc	Catiroc
Prod. Version	3A	3B	1	2A	1
TRL	9	9	9	8	5
Packages	PQFP240 TFBGA353	TQFP208	TQFP160	BGA400	TQFP208
Detector Compliant	- MA-PMT - PMT - PMT arrays - SiPM - SiPM matrices	- RPC - PMT - MAPMT	- micromegas - GEMs	- Si PIN diodes - Silicon strips	- PMT arrays - PMT - MA-PMT
Optimized for	MA-PMT	RPC	GEMs	Si PIN diodes	PMT arrays
Nb of channels	64	64	64	64	16
Measurements	- Self triggered - Ext trigger - Charge linear - Photon counting - Time (trigger)	- Self triggered - Ext trigger - Charge linear - semi digital 3 adjust. levels	- Self triggered - Ext trigger - Charge linear - semi digital 3 adjust. levels	- Self triggered - Ext trigger - Charge linear - Time (TDC)	- Self triggered - Ext trigger - Charge linear - Time (trigger) - Time (TDC)
Outputs	- 64 Triggers - Trigger OR - 1 mux charge analogue - ADC adjust. 8/10/12b	- Trigger OR - 1 mux charge analogue	- Trigger OR - 1 mux charge analogue	- Trigger OR - 1 mux charge analogue - ADC (10/12b) - TDC (10/12b)	- 16 Triggers - 16 Shapers - Trigger OR - ADC (10b) - TDC (10b)
Input Polarity	Negative	Negative	Negative	Positive	Negative
Applications **Main features**	Energy meas. Photon counting rate < 30MHz MA-PMT gain adj.	Energy meas. Time stamping Semi-digital out. 3-level trigger I2C bus	Energy meas. Time stamping Semi-digital out. 3-level trigger	Energy meas. Time stamping	Energy meas Time stamping System on chip Low dead time

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Summary

COMING SOON

	Spaciroc	Citiroc	Photoroc	Petiroc	Triroc
Prod. Version	3	1A	Available soon	2A	1A
TRL	9	8	5	6	6
Packages	TQFP160	TQFP160 TFBGA353	PQFP240	TQFP208 TFBGA353	TFBGA353
Detector compliant	- MA-PMT - PMT arrays - PMT - SiPM	- SiPM - SiPM matrices	- MA-PMT - PMT	- SiPM - SiPM matrices	- SiPM - SiPM matrices
Optimized for	MA-PMT	SiPM	MA-PMT	SiPM	SiPM
Nb of channels	64	32	64	32	64
Measurements	- Self triggered - Photon counting	- Self triggered - Ext trigger - Charge (linear) - Time (trigger)	- Self triggered - Charge ToT - Photon counting - Time (trigger	- Self triggered - Charge linear - Time (trigger) - Time (TDC)	- Self triggered - Charge linear - Time (TDC)
Outputs	- Trigger OR - 8 sum charge - Counters (8bits)	- 32 triggers - Trigger OR - 1 mux charge analogue	- 64 triggers or - 64 ToT - Trigger OR	- 32 triggers - Trigger OR - 1 mux charge & Hit analogue & dig. - ADC (10b) - TDC (10b)	- Trigger OR - 1 mux charge & Hit analogue & dig. - ADC (10b) - TDC (10b)
Input Polarity	Negative	Positive	Negative	Positive Negative	Positive Negative
Applications **Main features**	Photon counting rate > 100MHz Internal counters Radiation tolerant Space application	Energy meas. Time of flight Photon counting Calibration input SPE spectrum Input DAC SiPM HV adjust.	Energy meas.(ToT) Photon counting rate < 70MHz Energy meas. ToT	Energy meas. Time of flight Time stamping Photon counting Input DAC SiPM HV adjust.	Energy meas. Time of flight Time stamping System on chip Input DAC SiPM HV adjust.

ToT : Time over Threshold – ADC : Analogue to Digital Converter – TDC : Time to Digital Converter – MA PMT : Multi-Anode Photomultiplier

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Maroc 3A

Photomultiplier-tubes read-out chip

MAROC3A is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron (50fC) and a charge measurement up to 30 photoelectrons (~ 5 pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 4 thanks to an 8 bit variable gain preamplifier allowing to compensate the non-uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5 pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths: one made of a bipolar or unipolar fast (15 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1 pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit Wilkinson ADC.

Detector Read-Out	MAPMT, SiPM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron with a 10^6 PM gain or 50 fC
Timing Resolution	60ps RMS on single photo-electron, threshold 1/3 of photo-electron
Dynamic Range	5 pC (10^6 PM gain), Integral Non Linearity: 2% up to 5 pC
Packaging & Dimension	PQFP240, TFBGA353
Power Consumption	3.5 mW /ch, power supply= 3.5V
Inputs	64 current inputs
Outputs	64 trigger outputs Wired OR of the 64 triggers for each of the 2 discriminators 1 multiplexed analog charge output that can be daisy chained 1 digital charge measurement (8, 10 or 12 bits)
Internal Programmable Features	gain adjustment between 0 and 2 over 8 bits for each input preamp, trigger threshold adjustment (10bits), analog and digital charge measurement, 64 trigger outputs, 64 trigger masks

They are using Maroc 3A

CERN (ATLAS luminometer)
Jefferson lab (CLASS12)
Industrial applications under NDA

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Maroc 3A

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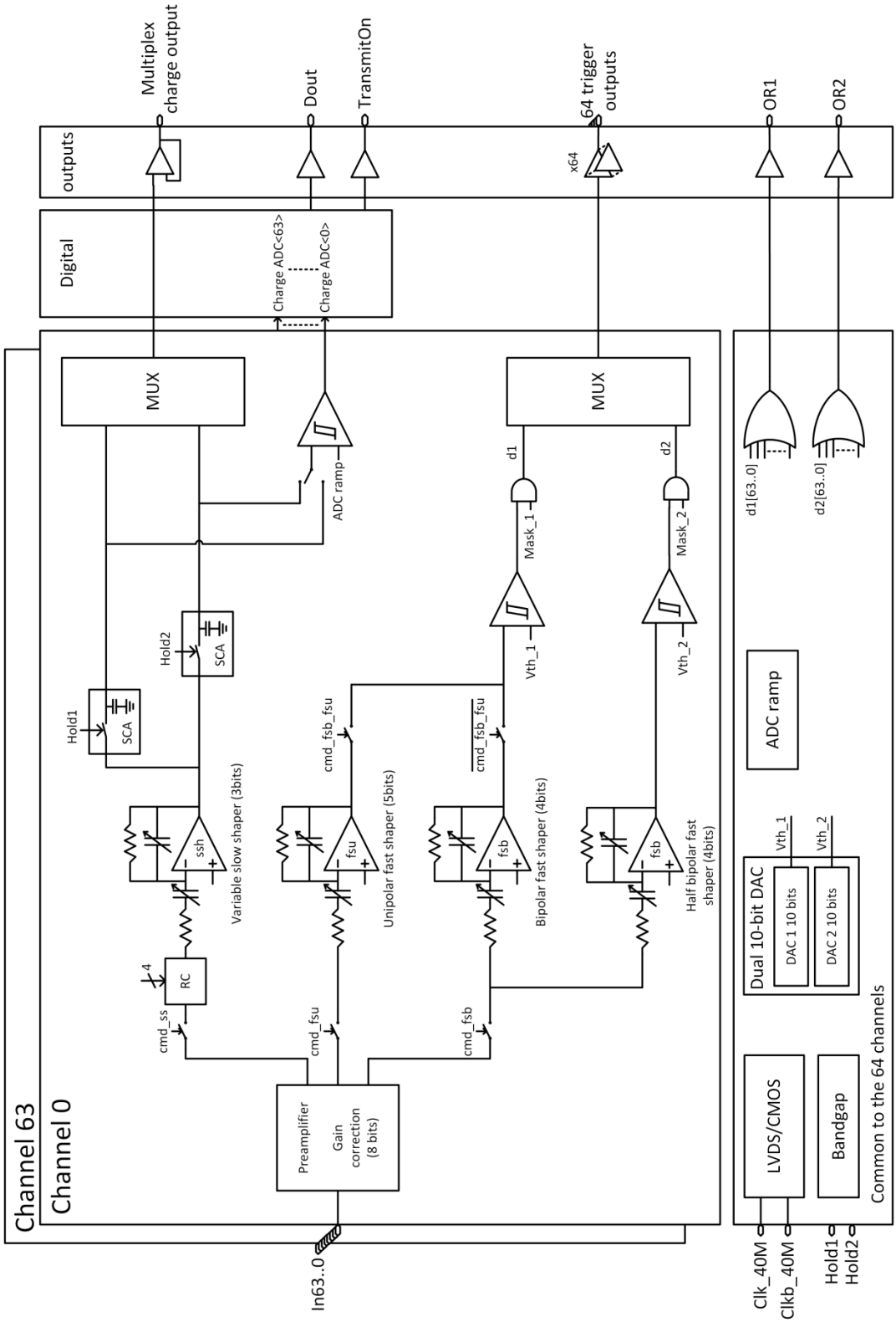
Maroc 3A

Photomultiplier-tubes read-out chip



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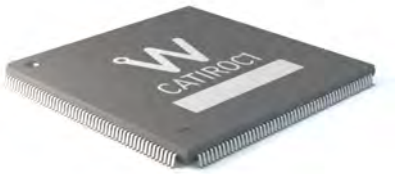
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip

CATIROC 1 is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs) in large scale applications such as water Cerenkov experiments. The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell for large area of detection.

An adjustment of the gain of each channel compensates for the gain variation of the PMTs and allows using only one HV cable for the 16 PMTs. In the ASIC, the 16 channels are totally independent. In each channel, the auto-trigger starts the charge and time measurements which are then converted and stored. Only the hit channels are read out by one serialized output. The time measurement is done by a 26-bit counter at 40 MHz for the coarse time and a Time to Amplitude Converter (TAC) for the fine time, giving a resolution of 200ps RMS. The charge measurement is done by a dual gain preamplifier followed by a shaper with variable shaping times (25 ns, 50 ns or 100 ns). Charge and fine time values are converted by a 10 bit ADC.



Moreover CATIROC 1 can be used as an analogue front-end ASIC for PMTs. The 16 triggers and 16 shapers output can be used in an application specific optimized front-end board.

Detector Read-Out	PMT, PMT array
Number of Channels	16
Signal Polarity	Negative
Sensitivity	Trigger on one third of photo-electron on each channel
Timing Resolution	200ps RMS on single photo-electron
Dynamic Range	400 photo-electrons (10^6 PMT gain) Integral Non Linearity 1% up to 400 p-e
Packaging & Dimension	TQFP208
Power Consumption	Power supply: 3.3V 21mW/ch.
Inputs	16 voltage inputs
Outputs	16 trigger outputs 16 shaper output 1 or of the 16 trigger output 1 serialized digital data output (50bits/channel)
Internal Programmable Features	16 channel gain adjustment (16x8bits), trigger and gain threshold adjustment (2x10bits), charge measurement tuning, 16 trigger masks, channel by channel trigger output enable.

They are using Catiroc 1

JUNO experiment
WA105 collaboration

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Catiroc 1

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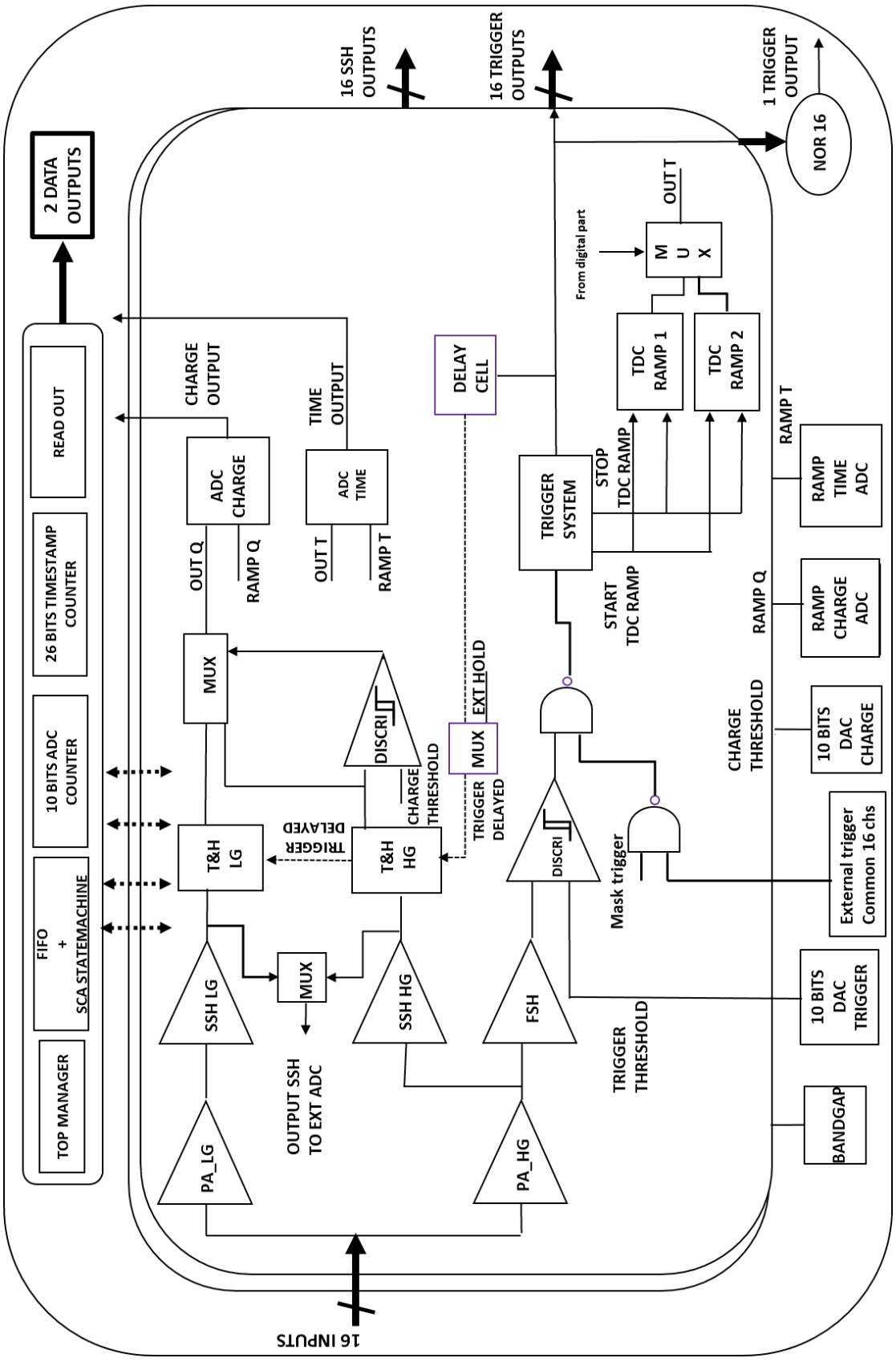
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip



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Spaciroc 3

Photomultiplier Tubes Photon Counting Read-Out-Chip

Spaciroc 3 is a 64-channel chip reading out negative fast input current pulses such as those provided by Multi Anode Photo Multipliers for space-borne and low-power applications. Spaciroc 3 counts photon individually within a Gate Time Unit (GTU).

The 64 inputs from MAPMT Anodes are read-out by a current amplifier followed by a discriminator. Threshold of that discriminator is set by a 10b DAC and an individual 7b DAC to compensate for the non-uniformity between detector channels. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron. The digital part operates continuously and handles data conversion of each Photon Counting channel. The digital data are transmitted through a dedicated parallel communication links within the defined Gate Time Unit (GTU). The ASIC data output rate is 40 MHz. Spaciroc 3 is radiation tolerant and its power consumption is lower than 1 mW/channel.

Detector Read-Out	SiPM, MAPMT
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron or 50 fC with a 10^6 PM gain
Timing Resolution	Not relevant
Dynamic Range	Min Gate Time Unit 1.6us, max count 255 per GTU - Photon counting rate > 100MHz
Packaging & Dimension	TQFP160
Power Consumption	< 1 mW /ch, power supply: 3V
Inputs	64 current inputs
Outputs	8 serial data outputs (8b) for photon counting
Internal Programmable Features	Trigger threshold adjustment (10b), Individual threshold (7b)

They are using Spaciroc 3

CNES (EUSO Ballon, flight 2014)
NASA (EUSO-SPB)
NASA (Mini EUSO)

More about Spaciroc 3

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

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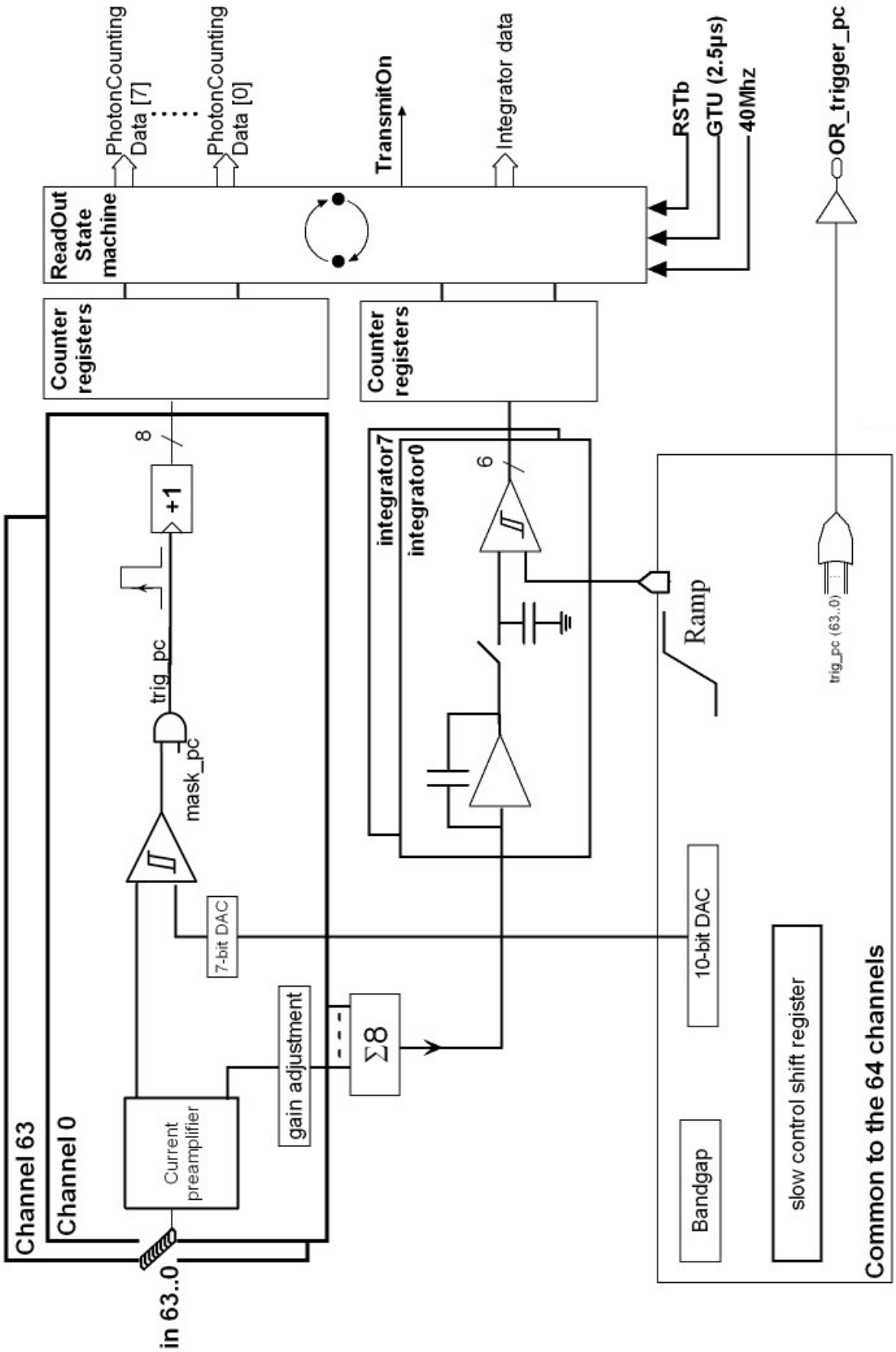
Spaciroc 3

Photomultiplier Tubes Photon Counting Read-Out-Chip



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Citiroc 1A

Scientific instrumentation SiPM read-out chip

Citiroc 1A is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for scientific instrumentation application.

Citiroc 1A allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc 1A outputs the 32-channel triggers with a high accuracy (better than 100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs. Citiroc 1A can be calibrated using a unique calibration signal.

Timing measurement better than 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 p.e. The power consumption 225mW with all stages on.

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP 160 – TFBGA353
Power Consumption	225mW – Supply voltage : 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 2 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

They are using Citiroc 1A

INAF – IASF (CTA experiment)
CERN (Baby mind experiment)

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Citiroc 1A

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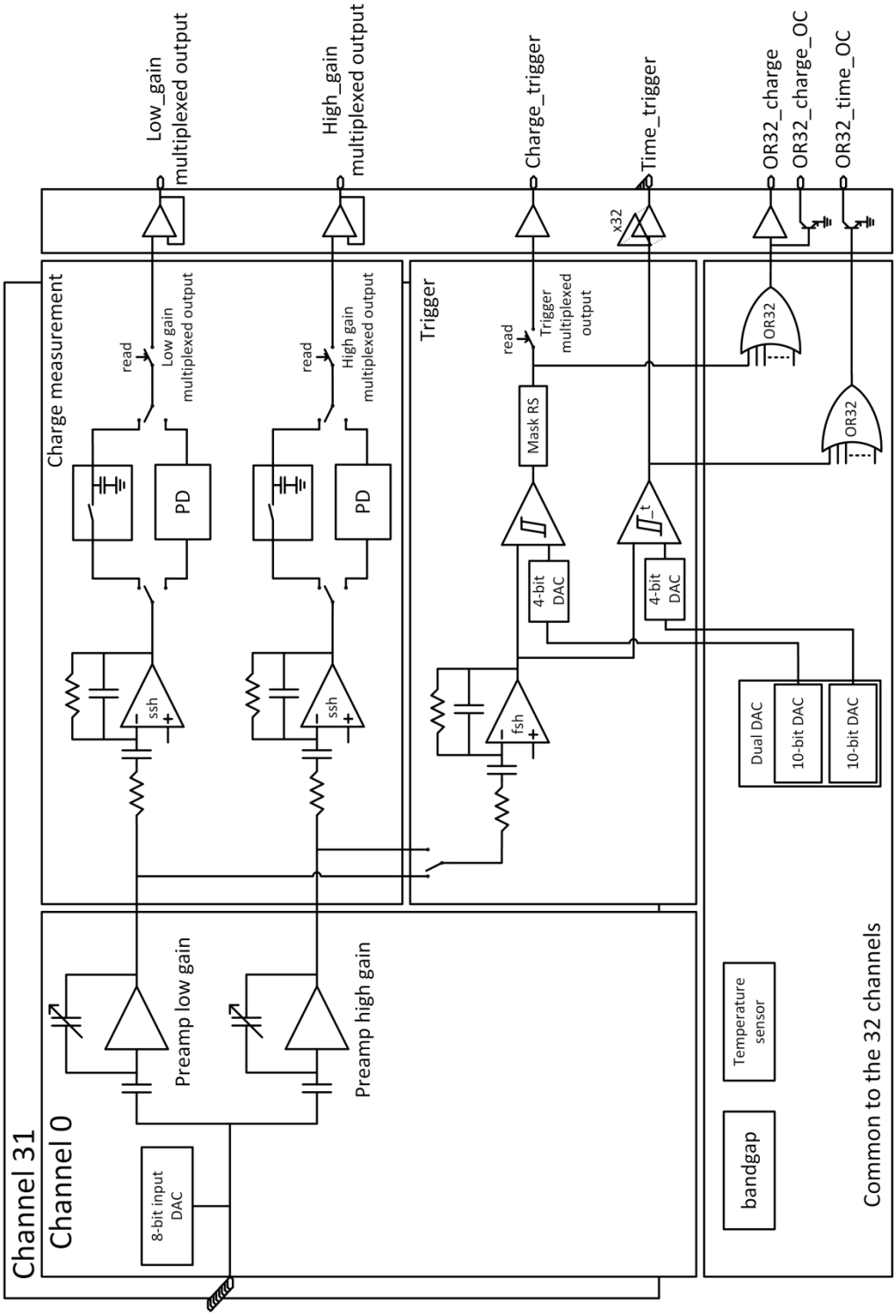
Citiroc 1A

Scientific instrumentation SiPM read-out chip



SSH – Slow Shaper ; FSH – Fast Shaper; PD – Peak Detector

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Petiroc 2A

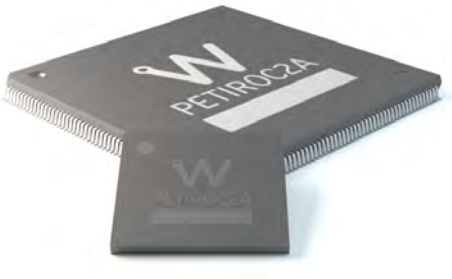
SiPM read-out for time-of-flight PET

Petiroc 2A is a 32-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Petiroc 2A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 40ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6 mW/channel, excluding buffers used to output the analogue signals. The main application of Petiroc 2A is PET time-of-flight prototyping but it can also be used for any application that requires both accurate time resolution and precise energy measurement.



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch

They are using Petiroc 2A

Industrial applications
Cannot be disclosed

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Petiroc 2

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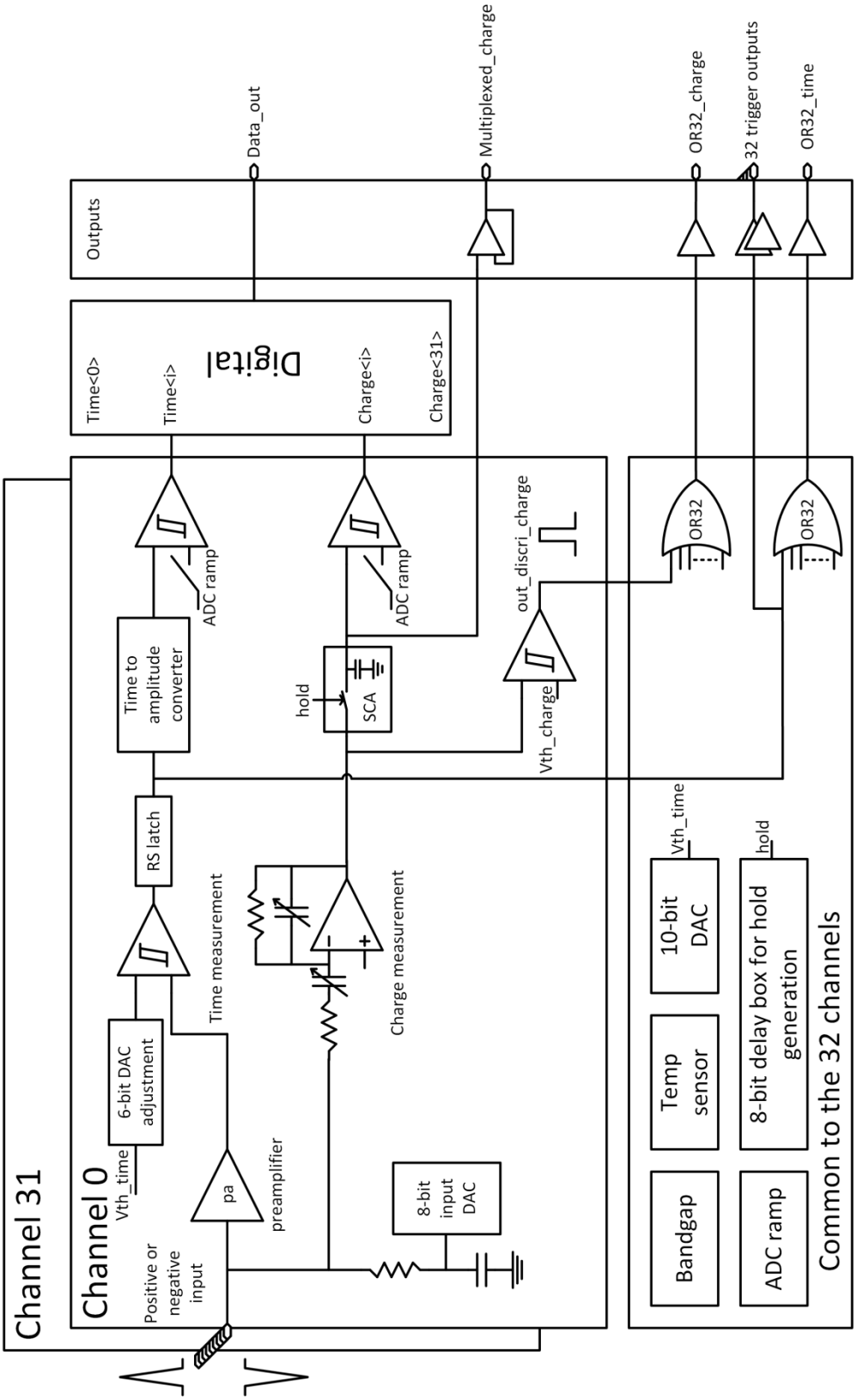
Petiroc 2A

SiPM read-out for time-of-flight PET



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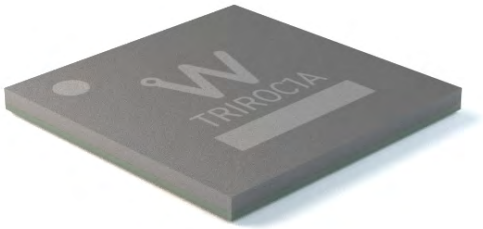
Triroc 1A

All-in-one SiPM read-out for multimodal PET inserts

Triroc 1A is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Triroc 1A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 30ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.



An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. The main application of Triroc 1A is PET time-of-flight but it can also be used for any application that requires both accurate time resolution and precise energy measurement. Triroc 1A is available in naked dies or BGA packaging (12x12mm, 353 balls).

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, trigger latch, Power Pulsing

They are using Triroc 1A

Trimage collaboration (PET/IRM/EEG)
Industrial application
Cannot be disclosed

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Triroc 1A

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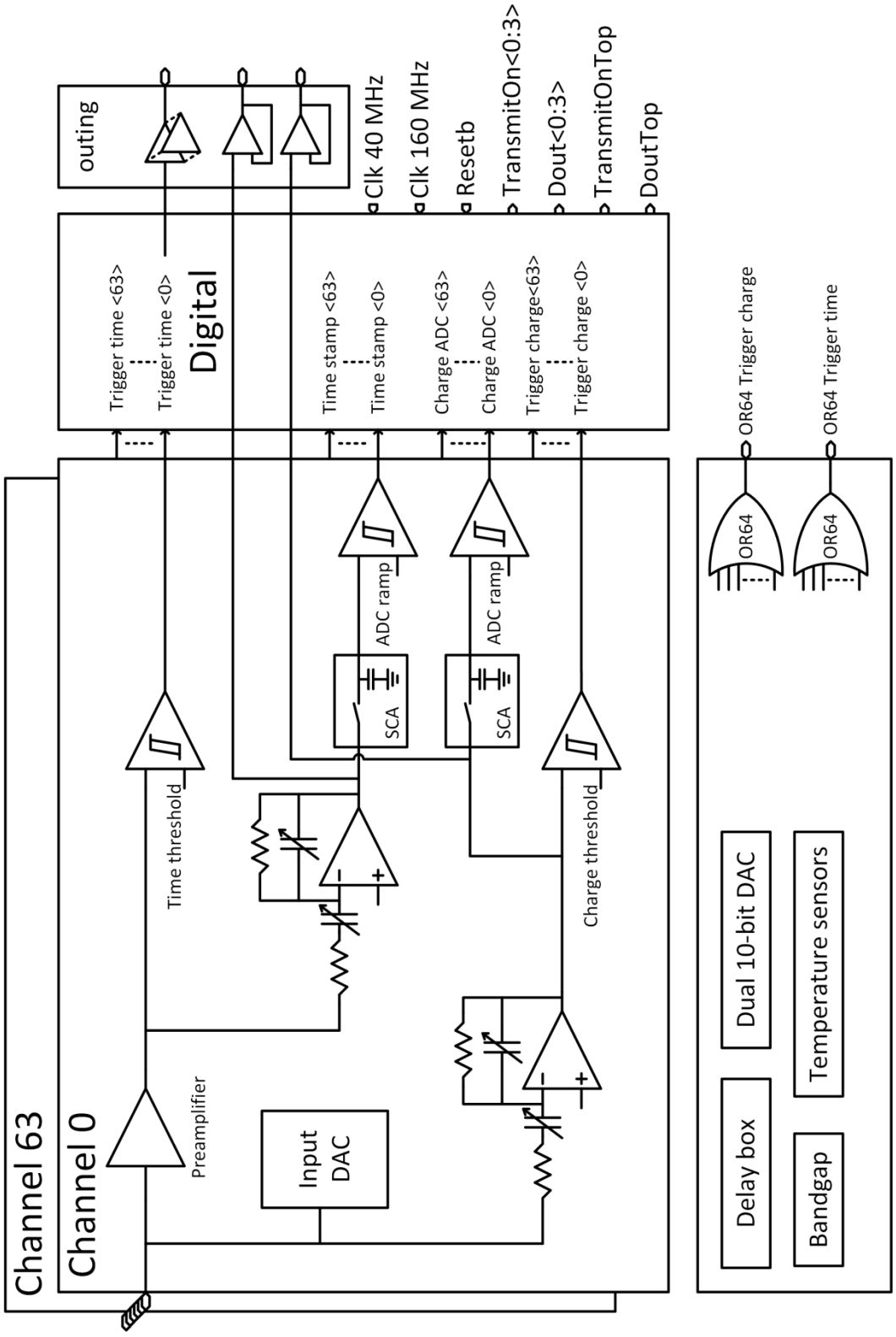
Triroc 1A

All-in-one SiPM read-out for multimodal PET inserts



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Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip

SKIROC 2A is a 64-channel front-end ASIC designed to readout silicon PIN diodes. Each channel is made of a variable-gain and low-noise charge preamplifier followed by two shapers – one with a gain of 1 and the other with a gain of 10 – to provide a charge measurement from 0.2 fC up to 10 pC. A time tagging is performed by a 12-bit TDC ramp. The charges and times are stored in a 15-depth Switched Capacitor Arrays (SCA), the values of which are converted by a multi-channel 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The analog value of the charge is also available on an output pin. The trigger chain is composed of a high gain fast shaper and a discriminator and allows each channel to auto trigger down to 0.2 fC. Thresholds of the 64 discriminators are set by a common 10-bit DAC and an individual 4-bit DAC per channel. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns) to provide the Hold signal for the SCA cells of the slow channel. The power consumption is 6.2 mW/channel and each stage can be individually shut down when not used. 616 slow control parameters are available to set various configurations and ensure the versatility of the chip.

Detector Read-Out	Si PIN Diodes
Number of Channels	64
Signal Polarity	positive
Sensitivity	Trigger on 0.2fC
Timing Resolution	N/A
Dynamic Range	10 pC, Integral Non Linearity <1%
Packaging & Dimension	BGA 400 (17x17mm)
Power Consumption	6.2 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	1 multiplexed analog charge output 12-bit charge and time measurement Trigger OR of the 64 discriminators
Internal Programmable Features	Common gain adjustment for the input, common trigger threshold adjustment (10 bits) and individual threshold (4 b), 12-bit charge and time measurement, 64 trigger masks, multiplexed analog output

They are using Skiroc 2A

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CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Skiroc 2A

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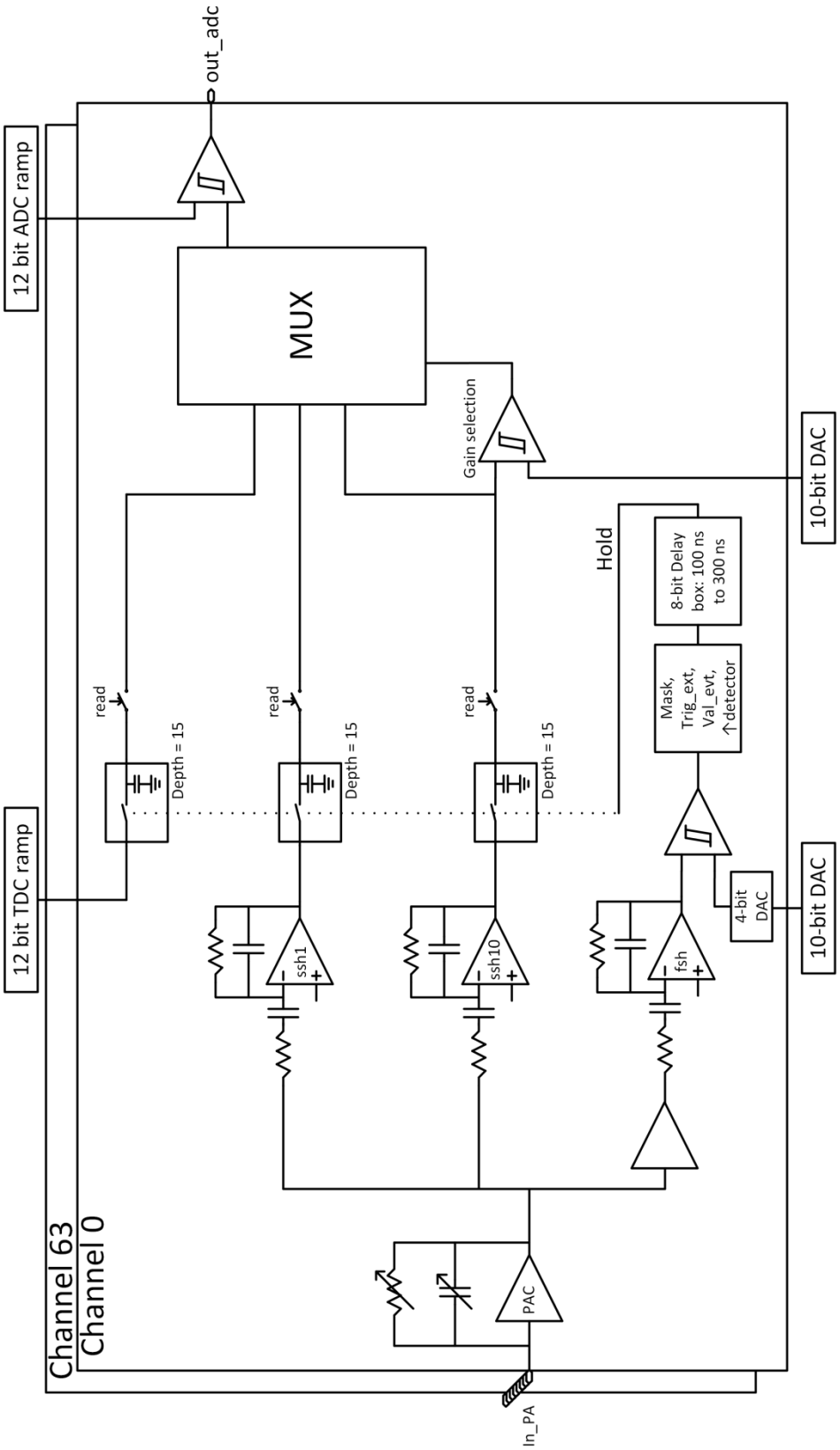
Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip



weeroc

Hardroc 3B

RPC and gaseous detector semi-digital read-out chip

HARDROC 3B is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from various detectors (Resistive Plate Chambers, Multi Anode Photo Multipliers, ...). HARDROC 3B provides a semi-digital readout with three thresholds tunable between 10 fC up to 10 pC and integrates a 8-depth digital memory per channel to store the 2 encoded outputs of the 3 discriminators upon channel trigger. The three thresholds are set by three integrated 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel is trigger-wise independent and can auto-trigger on signal down to 10 fC. A multiplexed charge measurement allows linear analogue measurement up to 30pC.

The power consumption is around 2.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.

Detector Read-Out	MAPMT, RPC
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 10 fC with 100% efficiency
Timing Resolution	Time stamping 200ns
Dynamic Range	30 pC
Packaging & Dimension	TQFP208
Power Consumption	2.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	gain adjustment between 0 and 2 over 8 bits for each input preamp, trigger threshold adjustment (10bits), 3*64 trigger masks, I2C programmable

They are using Hardroc 3B

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Hardroc 3B

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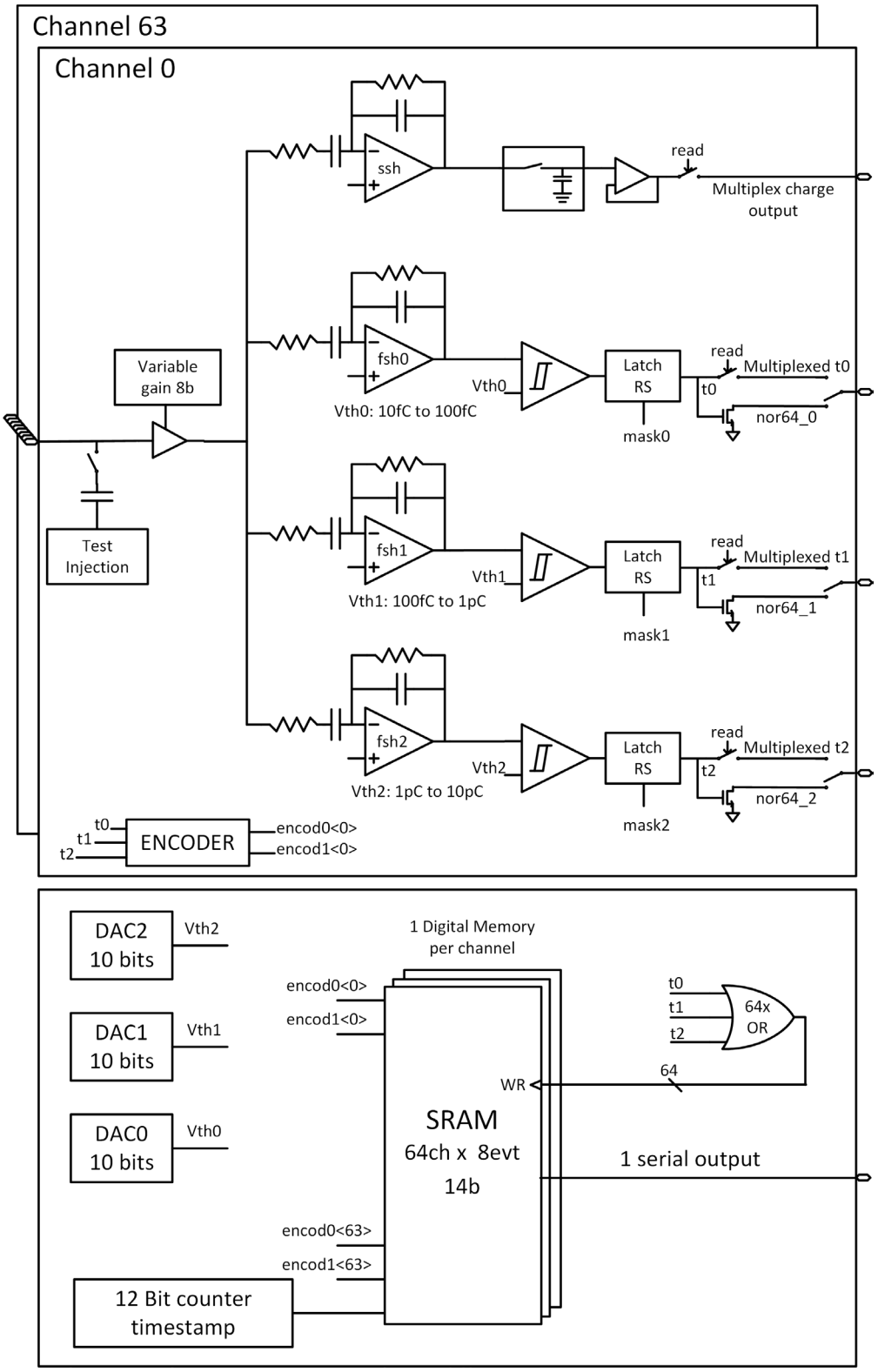
Hardroc 3B

RPC and gaseous detector semi-digital read-out chip



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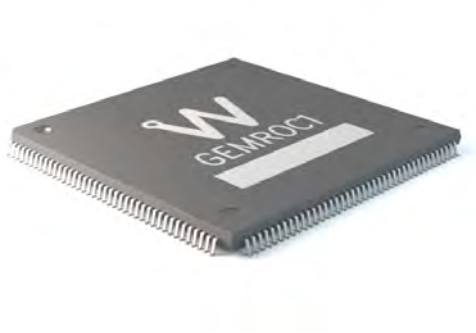
Gemroc 1

Micromegas and GEMs semi-digital read-out chip

GEMROC 1 is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from low gain detectors (GEMs, Micromegas, ...). GEMROC 1 provides a semi-digital readout with three thresholds tunable from 1 fC to 500 fC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the timestamp from a 24b counter. The three thresholds are set internally by three 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 1 fC input charge. A multiplexed charge measurement up to 500fC is integrated.

The power consumption is 1.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.



Detector Read-Out	Micromegas, GEM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger 1 fC
Timing Resolution	Time stamping 200ns
Dynamic Range	500 fC
Packaging & Dimension	TQFP160
Power Consumption	1.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	Trigger threshold adjustment (10bits), 3*64 trigger masks, multiplexed latched trigger or direct OR64 trigger outputs

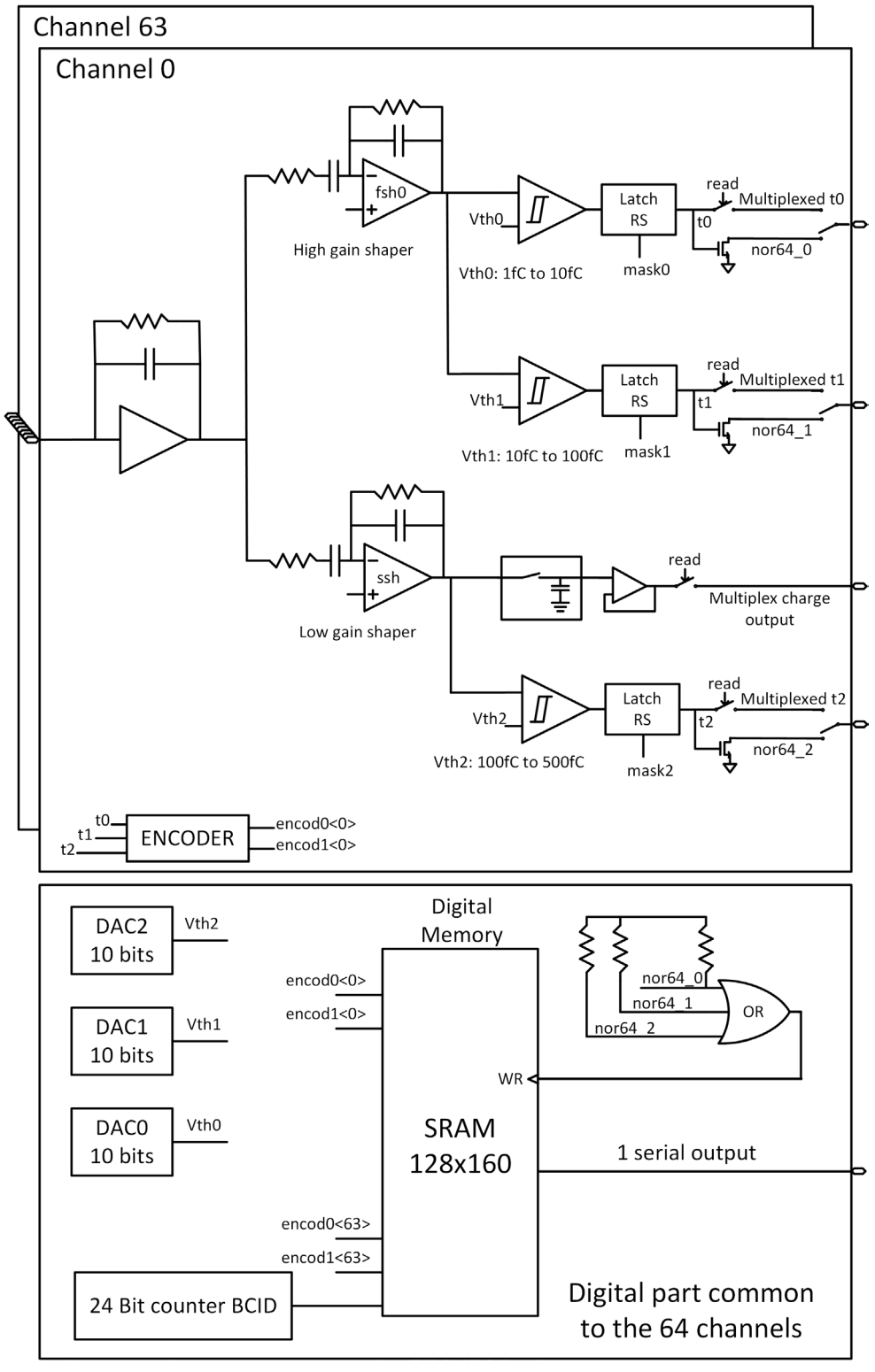
They are using Gemroc 1

Industrial application (NDA)

CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

More about Gemroc 1


Channel 63
Channel 0
fsh0
High gain shaper
Vth0
Vth0: 1fC to 10fC
Latch RS
mask0
read
Multiplexed t0
t0
nor64_0
Vth1
Vth1: 10fC to 100fC
mask1
Multiplexed t1
t1
nor64_1
ssh
Low gain shaper
Multiplex charge output
Vth2
Vth2: 100fC to 500fC
mask2
Multiplexed t2
t2
nor64_2
t0
t1
t2
ENCODER
encod0<0>
encod1<0>
DAC2 10 bits
Vth2
DAC1 10 bits
Vth1
DAC0 10 bits
Vth0
Digital Memory
encod0<0>
encod1<0>
nor64_0
nor64_1
nor64_2
OR
WR
SRAM 128x160
1 serial output
encod0<63>
encod1<63>
24 Bit counter BCID
Digital part common to the 64 channels

Small details
Great differences

CAEN
Tools for Discovery

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CAEN SpA

Via Vetraia 11
55049 - Viareggio • Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

CAEN GmbH

Klingenstraß e 108
42651 - Solingen • Germany
Phone +49.212.2544077
Fax +49.212.2544079
info@caen-de.com
www.caen-de.comt

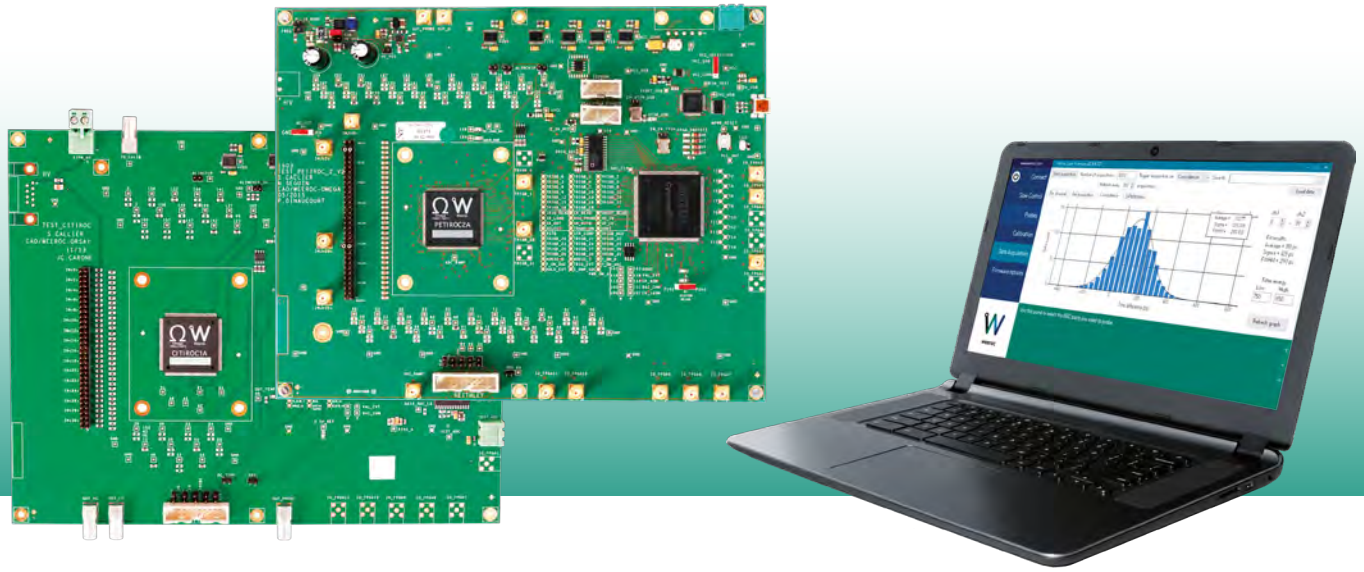
CAEN Technologies, Inc.

1140 Bay Street - Suite 2C
Staten Island, NY 10305 • USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

NEW

Weeroc Testboards

Control Systems for Weeroc ASICs



A simple way to learn the use of Weeroc ASICs

Features

- Specific design for each Weeroc ASIC
- Hosting a small ASIC for easy DAQ management
- Easy characterization and debug of the ASIC
- Access to all ASIC's digital and analog I/Os
- ASIC internal signals monitor
- Data acquisition with real detectors
- Connections for an external High Voltage power supply
- Mini-USB for data transfer and board power supply
- Control and acquisition software for Windows OS (LabVIEW interface for TRIROC 1A board)

Overview

Weeroc Testboards are compact form factor platforms designed to control and read out Weeroc ASICs. This tool is suited to easily evaluate the characteristics of the ASIC and, thanks to its features, allows a versatile use with real detectors. The testboard provides easy access to all ASIC's digital and analog I/Os and implements a DAQ system consisting of an Altera Cyclone III FPGA and 12-bit ADCs.

The board hosts connections for detectors and the relative High Voltage distribution lines. Moreover, it provides the possibility to inject signals in the ASIC analog inputs using a generator.

A dedicated software for each different ASIC is available. It provides a simple GUI to set all the programmable parameters of the ASIC and allows the user to perform calibration and DAQ in an intuitive way. Some firmware options can also be set in order to manage DAQ within an experiment..

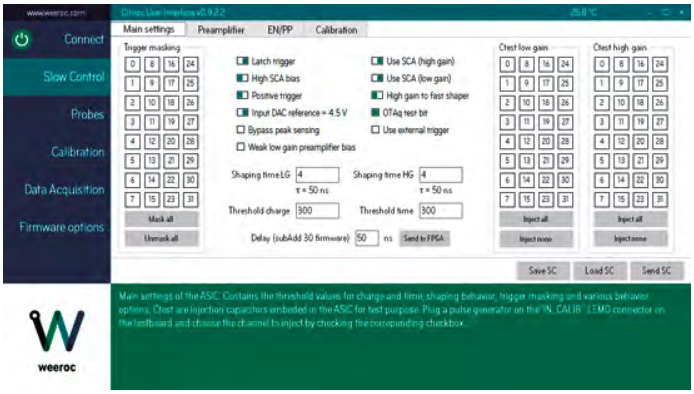
Software

Testboard Software

FREE

For each different testboard, a dedicated User Interface software for Windows OS is available for free download. It provides a simple GUI to set all the programmable parameters of the ASIC and allows the user to perform calibration and DAQ. Some firmware options can also be set.

The TRIROC testboard is equipped with a LabVIEW User Interface.



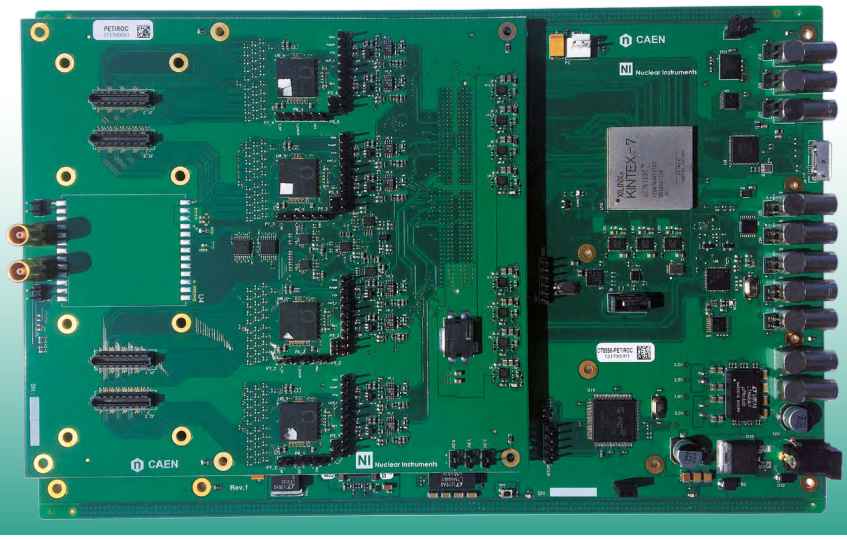
Ordering Option

Code	Description
WWTBCATIROC1	Testboard for CATIROC 1 chip
WWTBCITIROC1	Testboard for CITIROC 1A chip
WWTBGEMROC1A	Testboard for GEMROC 1 chip
WWTBHARDROC3	Testboard per HARDROC 3B
WWTBMAROC3AA	Testboard for MAROC 3A chip
WWTBPETIROC2	Testboard for PETIROC 2A chip
WWTBPHOTORC1	Testboard for PHOTOROC 1A chip
WWTBTRIROC1A	Testboard for TRIROC 1A chip

NEW

DT5550W

Weeroc ASICs Development System



Develop your DAQ system with Weeroc ASICs and the user programmable FPGA

Features

- Designed to be compatible with a wide selection of Weeroc ASICs for different types of detectors (SiPM, PMT, GEM, etc.)
- Open FPGA for user custom application
- Default firmware and control software to read out supported Weeroc ASICs and perform basic measurements with detectors
- Availability of external sensor adapter and HV power supply for SiPMs
- 8 analog acquisition channels, 14-bit 80 MS/s ADC to monitor ASIC outputs
- Programmable low jitter (less then 1 ps) clock source as reference for on chip TDC
- SPI and I2C controller for ASIC configuration
- USB 3.0 bus for fast data transfer
- 8 general purpose digital I/Os on LEMO Connectors for DAQ control signals (external trigger, busy, etc.)
- Fully supported by SCI-Compiler, graphical FPGA programmer for user application development (LICENSE INCLUDED)

WW55PETI2AA4 - PETIROC Piggyback Board

As an example of piggyback, the PETIROC board A55PET4 hosts 4 PETIROC chips offering to the user the possibility to read out 128 SiPM detectors. The board can be fitted with CAEN A7585D HV module to bias up to 2 matrices (64 channels), connected directly on the board, with the possibility to use an external adapter and an extension cable to arrange the two detectors in several geometries.

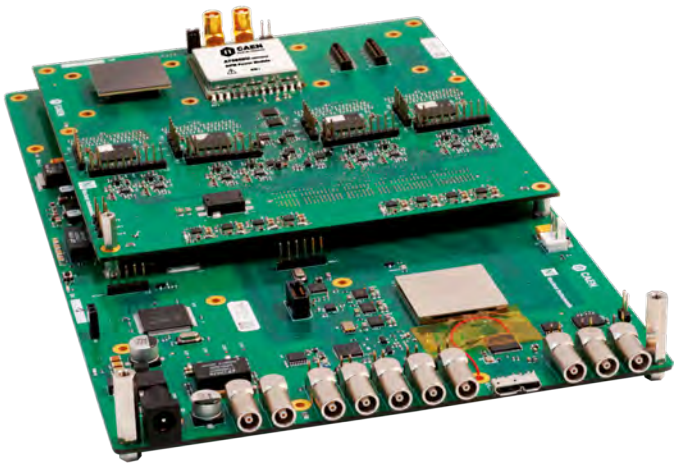
SCI-5550W Readout Software is available to control up to 4 PETIROC ASICs and the SCI-Compiler tool can be used to program the board FPGA for user custom applications. See front-end electronics and power supplies for SiPM section for more details.

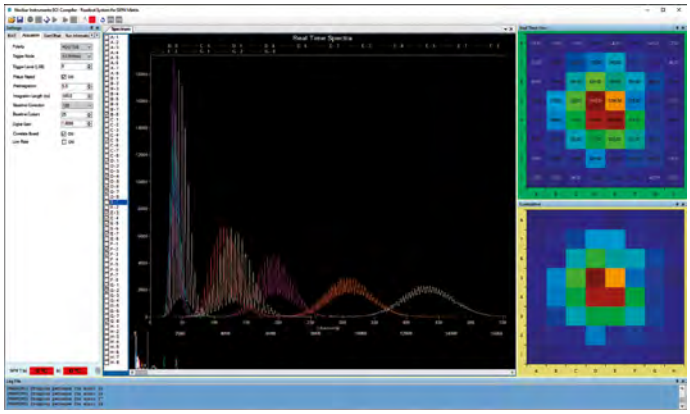
Overview

The DT5550W is a development and DAQ platform with programmable FPGA designed to read out Weeroc ASICs. This tool offers a complete solution to evaluate the characteristics of the ASIC and develop a ready-to-use experimental system for a wide variety of detectors (SiPMs, PMTs, GEMs, etc.). The full system is composed by two boards: a motherboard with an FPGA, USB 3.0 connectivity, power supply, ADCs and a replaceable piggyback board that hosts 1,2 or 4 Weeroc ASICs, detector connectors and high voltage power supply (if using SiPMs).

The DT5550W architecture allows to adapt, in a simple and intuitive way, the hardware acquisition to the user configuration: more than 200 digital signals interconnect the piggyback boards with the motherboard to read out and monitor all the signals from the ASICs with the FPGA. The DT5550W has an onboard 8 channels 14-bit 80 MS/s simultaneous sampling ADC to monitor analog outputs from the chip.

A default firmware is provided for each supported ASIC, allowing the user to read-out multiple ASICs and perform basic energy and time measurements with supported detectors.





DAQ control software for DT5550W with PETIROC piggyback board.

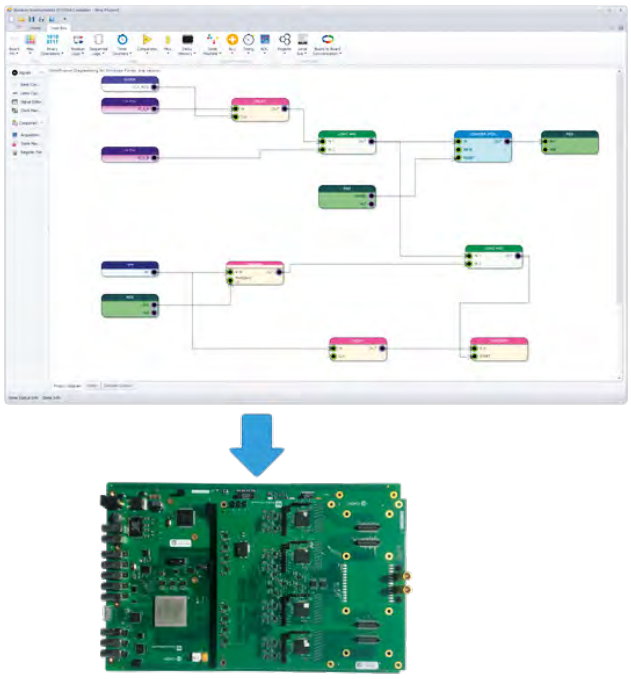
Software

SCI-5550W Readout Software

FREE

An open source control software with GUI for Windows is distributed as readout software and as example to implement more complex systems. The GUI allows the user to:

- Configure the ASICs
- View realtime energy spectra
- Make imaging with detector matrices (e.g.SiPM matrices)
- View time distribution plot with respect of one channel
- Dump on file all data in output of the ASIC in binary or JSON format



Software

SCI-Compiler

SCI-COMPILER CAEN

LICENSE INCLUDED

DT5550W includes the SCI-Compiler software, a graphic tool for FPGA programming which allows the user to realize a customizable readout logic. All functions to configure the ASIC (from firmware or from PC), to read out the ASIC, to route the trigger to the FPGA are directly implemented in the “Weeroc” Palette. The software generates the VHDL source code, C/C++/C#/Python libraries, drivers and example code (to be used in Windows, Linux and MacOS) to help integrating the firmware automatically without requiring to be a VHDL expert.

Ordering Option

Code	Description	
WDT5550WXAAA	DT5550W - WeeROC ASICs Evaluation and DAQ System	
WW55PETI2AA1	A55PET1 - Piggyback Board with 1 PETIROC chip	
WW55PETI2AA2	A55PET2 - Piggyback Board with 2 PETIROC chip	
WW55PETI2AA4	A55PET4 - Piggyback Board with 4 PETIROC chip	
WW55CITI1AA2	A55CIT2 - Piggyback Board with 2 CITIROC chip	COMING SOON
WW55CITI1AA4	A55CIT4 - Piggyback Board with 4 CITIROC chip	COMING SOON
WW55CATI1AA1	A55CAT1 - Piggyback Board with 1 CATIROC chip	COMING SOON
WW55MAROC3A1	A55MAR1 - Piggyback Board with 1 MAROC chip	COMING SOON
WW55PHOTO1A1	A55PHO1 - Piggyback Board with 1 PHOTOROC chip	COMING SOON
WW55GEM1AAA1	A55GEM1 - Piggyback Board with 1 GEMROC chip	COMING SOON
WA7585DXAAAA	A7585D - Digital Controlled Power Supply for SiPM 85V/10mA	

NEW

DT5702 - A1702

32 Channel Silicon Photomultipliers Readout Front-End Board

A compact ASIC-based solution to readout SiPM arrays with coincidence trigger logic

Features

- Based on Weeroc CITIROC 1A ASIC
- Amplification and shaping of the SiPMs output pulse
- Provides bias voltage in the range of 20-90 V individually adjustable for each channel
- Discrimination of shaped signal at configurable level from 0 to 50 SiPMs photo-electrons
- Provides basic coincidence of signals from each pair of adjacent even-odd channels
- Timing resolution up to 1 ns
- Formation of two independent timestamps
- Lemo I/O for time reference and control signals
- DAQ and control software with data output in ROOT format
- Daisy chain of up to 256 boards into one network interface
- Multiple boards event validation
- Efficient back-end communication based on Ethernet standard
- Trigger-independent firmware available (NEW)

Overview

The DT5702/A1702 is a compact 32-channels Front-End Board (FEB) designed to perform energy and time measurements with SiPM arrays. Given the increasing use of SiPMs in physics experiments, this solution is a valid approach for a variety of applications thanks to its flexibility, compact form factor and channel density.
The board provides adjustable bias voltage to the detectors and is able to process and digitize the analog signals.
The analog input signal is processed by a Weeroc CITIROC 1A ASIC providing charge amplifier with configurable gain, fast shaping with the peaking time of 15 ns for trigger formation and slow shaping with configurable peaking time in the range of 12.5 ns to 87.5 ns for amplitude measurements. Thanks to these features the DT5702/A1702 has a wide range of possible applications: from veto systems of neutrino experiments to SiPM arrays imaging.
The triggering logic is realized by a XILINX Spartan-6 FPGA. A trigger independent firmware is available by ordering option, useful to extract triggering pixel positional information, improve timing resolution and estimate the time walk.
The communication interface of the board is a 3-port Ethernet switch, which allows connection to a host computer and daisy chain of multiple boards.

The board is also available in boxed (DT5702) and naked (A1702) version.

A1702 - Front-End Board.

Ordering Option

Code	Description
WA1702XAAAAA	A1702 - 32-channel SiPM readout Front-End Board
WDT5702XAAAA	DT5702 - 32-channel SiPM readout Front-End Board BOXED

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Electronic Instrumentation

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High-end Microelectronics Design