

# An Ultralow-Power Switched Opamp-Based 10-B Integrated ADC for Implantable Biomedical Applications

G. Bonfini , A. S. Brogna, C. Garbossa , L. Colombini, M. Bacci,  
S. Chicca , F. Bigongiari, N. C. Guerrini , and G. Ferri

**Abstract** — This paper describes an ultralow-power switched opamp-based integrated analog-to-digital converter (ADC) for cardiac pacemakers applications. The ADC consumption, measured on 10 chip samples and averaged, is  $8.18 \mu\text{W}$  (stand-by value:  $1 \text{ nW}$ ) for the analog part and of  $9.71 \mu\text{W}$  ( $5 \text{ nW}$ ) for the digital one, using a supply battery of  $2.8 \text{ V}$ . The converter has a resolution of 10-b, its typical operating clock frequency is  $32 \text{ KHz}$  ( $2.9 \text{ KS/s}$  sampling rate) and is able to reach the same resolution at  $2 \text{ V}$  ( $0.7 \text{ KS/s}$  sampling rate), with a dissipation of  $1 \mu\text{W}$  and  $1.3 \mu\text{W}$  for analog and digital part, respectively.

**Index Terms** — Analog-to-digital converter (ADC), biomedical applications, low-power, switched-opamp.

## I. INTRODUCTION

In cardiac pacemakers, interface electronics is fundamental for obtaining information about heart functionality. The processing of a cardiac signal typically needs low-voltage, low-noise analog interfaces showing a very low power consumption and performing a suitable analog-to-digital conversion (ADC). The sense amplifier, which detects cardiac waveforms, cannot utilize switched capacitors (SC) because, at low supply voltages, complementary switches and op-amps do not efficiently work, due to the insufficient switch overdrive [1]. These problems can be solved by the use of a switched-opamp (SOA) technique that overcome the typical impairments of low-voltage, low-power systems [2]-[7]. This paper describes an SOA implementation of a cyclic algorithmic ADC showing a very low power consumption. The architecture has been implemented taking into account the typical constraints of a biomedical implantable applications: ultralow-current consumption (lower than  $5 \mu\text{A}$ ), with a typical power supply voltage of  $2.8 \text{ V}$  (but the ADC maintains its performance at  $3.5 \text{ V}$  and remains “on” also at only  $2 \text{ V}$  supply). The circuit has been fabricated in AMS BiCMOS  $0.8\text{-}\mu\text{m}$  BYQ technology and integrated in a 84 pin ceramic package.

## II. ADC ARCHITECTURE

The main aim of this paper is the design of an integrated ultralow-power (ULP) consumption ADC operating with a standard battery supply for cardiac pacemaker applications (operating from  $3.5 \text{ V}$  down to  $2 \text{ V}$ ) and having a resolution of 10 b, a conversion rate of  $2.9 \text{ KS/s}$ , an input dynamic range of  $800 \text{ mV}$ , low offset, no missing code, and a reduced silicon area. These performances have been obtained using a cyclic algorithmic approach with the SOA technique. The choice for this architecture instead of others [11] is motivated by the fact that SOA goals are not only the capability

---

Manuscript received January 29, 2003; revised September 25, 2003. This paper was recommended by Guest Editors A. Rodríguez-Vázquez, F. Mediero, and O. Feely.

G. Bonfini and A. S. Brogna are with the Dipartimento di Ingegneria dell'Informazione Università degli Studi di Pisa, 56122 – Pisa, Italy.

C. Garbossa , L. Colombini, M. Bacci, S. Chicca and F. Bigongiari are with Aurelia Microelettronica S.p.A.- C.A.E.N S.p.A. Company, 56023-Navacchio (Pi), Italy.

N. C. Guerrini , and G. Ferri are with the Dipartimento di ingegneria Elettrica, Università degli Studi di L'Aquila, 67040, L'Aquila, Italy (e-mail: [ferri@ing.univaq.it](mailto:ferri@ing.univaq.it)).

of reducing the supply voltage but also overcoming the limits connected with the switches overdrive. In fact, we also consider the possibility of completely turning “on” opamps only in one of the two phases of the main clock, with the opamp switched off in the other phase, so the power consumption of the entire system can be halved.

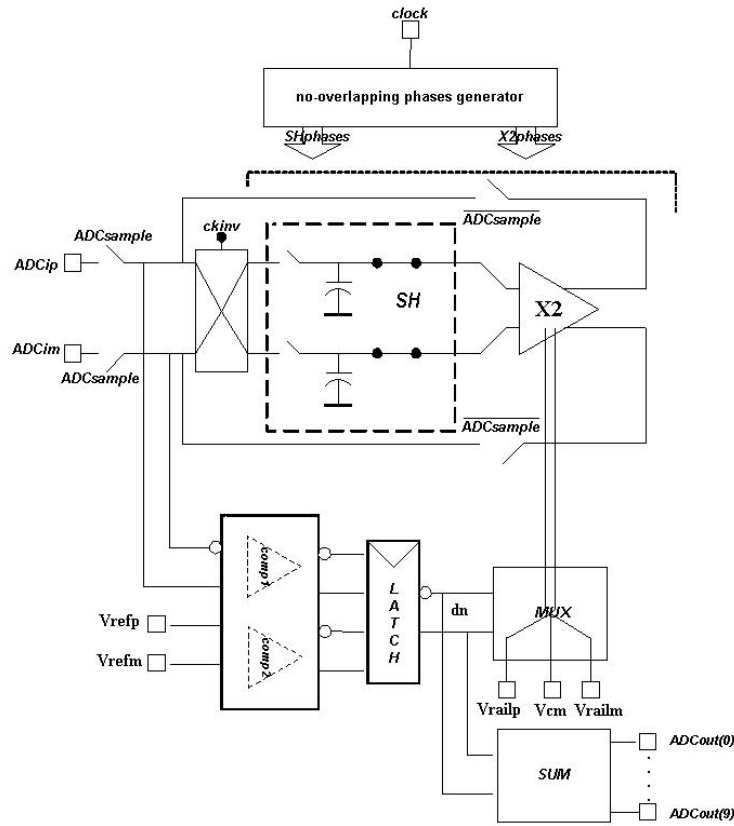


Fig. 1. ADC schematic diagram

Fig. 1 shows the system that implements the fabricated ADC. Its architecture is a classical cyclic/algorithmic topology with 1.5 b per cycle, made by three main blocks: a Sample and Hold (SH in Fig. 1), some comparators and a Multiplying DAC (X2). The ADC works as follows: when  $ADCsample$  is asserted (see Fig. 1), any analog signal coming from  $ADCip$  and  $ADCim$  is converted by two comparators (that act as a flash sub-ADC) in a 2-b digital number and sampled through the input switches of SH during the first phase (*phase1* in Fig. 2); then,  $ADCsample$  is removed and the SH block holds the sampled signal while X2 samples it. At this time, the input switches are opened, and a loop is created between X2 and SH. During the following clock cycles (*phase1-phase2*), the operation continues: the SH block samples the X2 output feedback, this signal is compared by two comparators, and the X2 block multiplies the SH output by two. If necessary, a reference voltage is added or subtracted to it, according to the result of the comparison. The ADC needs 11 clock cycles (32 kHz) to produce a 10-b output code. A new conversion begins (and a new input analog signal is processed) when  $ADCsample$  becomes active again. If  $V_{in}$  is the voltage difference between the inputs of SH,  $V_{ref}$  is the voltage reference ( $V_{ref} = V_{railp} - V_{railm}$ ),  $V_{resn}$  is the voltage residue at X2 output of  $n$ th conversion cycle and  $d_n$  is the respective binary code, then, for each cycle clock, the algorithm works as follows:

$$V_{resn} = \begin{cases} 2V_{in} - V_{ref} & \text{if } V_{in} > V_{ref}/4 & d_n = 10 \\ 2V_{in} & \text{if } -V_{ref}/4 \leq V_{in} \leq V_{ref}/4 & d_n = 01 \\ 2V_{in} + V_{ref} & \text{if } V_{in} < -V_{ref}/4 & d_n = 00 \end{cases}$$

Digital result  $d_n$  is the input of the block SUM that encodes the output. The SOA technique, traditionally used to reduce the operating supply voltage [9], in this case is mainly used to obtain a

reduced power consumption, for a 2 V minimum supply: in fact, if SH is “on”, X2 is “off” and vice versa. When a block is in OFF phase, the SOA output stage is in the high impedance condition and is pulled to  $V_{cm}$  by the related switches.

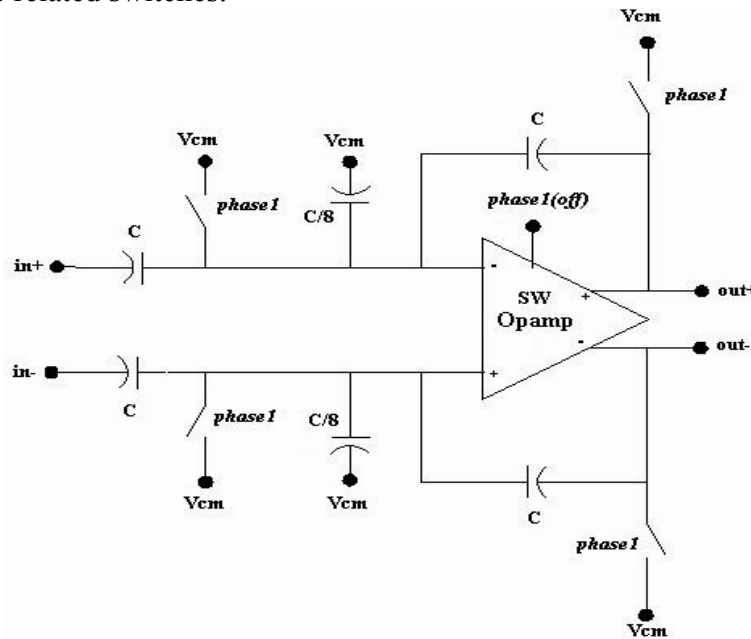


Fig. 2. SH architecture

Fig. 2 shows the SH architecture employed in this design. Its circuits consist of switches (in a transmission gate configuration), an SOA, two sample capacitors  $C$ , two hold capacitors  $C$  having the same value of the sample capacitors, and two capacitors having a value of  $C/8$  that avoid large spikes on the virtual ground and represents a tradeoff on the offset that these capacitors produce. Moreover, thanks to capacitance values and leakage specifications from the foundry, voltage drops due to leakage problems are negligible. During *not phase 1* (sample phase), the charge is stored on sampling capacitors  $C$ , and the SOA output stage is in the high impedance. In order to minimize the delay caused by slew-rate, the SOA output stage is pulled in this phase in the middle of the dynamic output range ( $V_{cm}$ ). During *phase 1*, the inputs of this stage are pulled to  $V_{cm}$  (while the output of the X2 stage is pulled to  $V_{cm}$ ), and then, the SOA is turned “on”, and all the switches are turned “off”. As a consequence, the charge is stored on the sampling capacitors of the X2 stage.

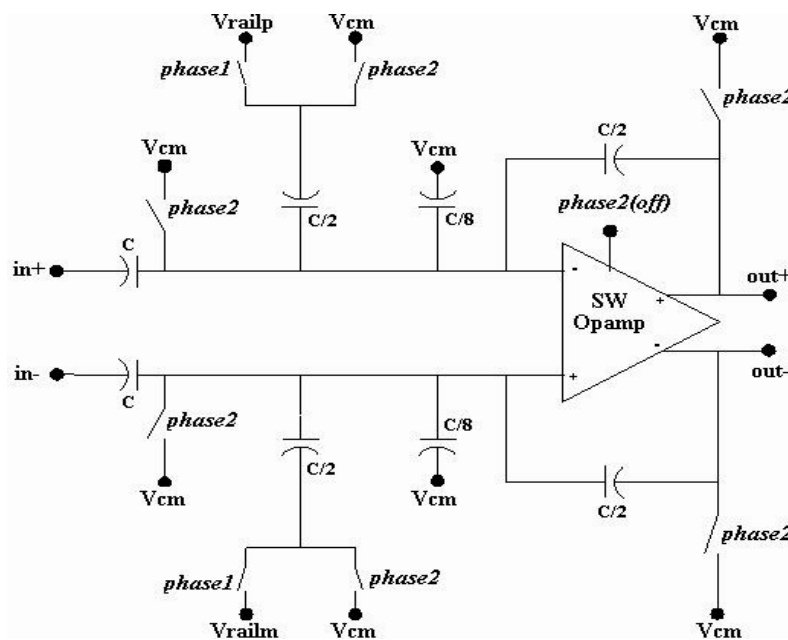


Fig. 3. X2 architecture

Fig. 3 shows the X2 architecture. In order to obtain a 1.5-b requirement, in the X2 stage, there are two capacitors with the same value of the hold capacitors ( $C/2$ ). During *phase2*, the charge is stored on the sampling capacitors (through the hold phase of the SH stage) and  $C/2$  input capacitors are pulled to  $V_{com}$  (as in the output stage of the SOA). At the end of the *phase2*, the amplifier is turned “on”. During the following phase (*phase1*), the  $C/2$  input capacitors are pulled to  $V_{rail}$  voltages, selecting comparing previous voltage residue and references ( $\pm V_{ref} / 4$ ) and the charge is stored on SH sampling capacitors. It is worth noting that 0.5-b redundancy operation is obtained using only two nonoverlapping phases (*phase1-phase2*) and the inverted ones (all switches are implemented by transmissions gate).

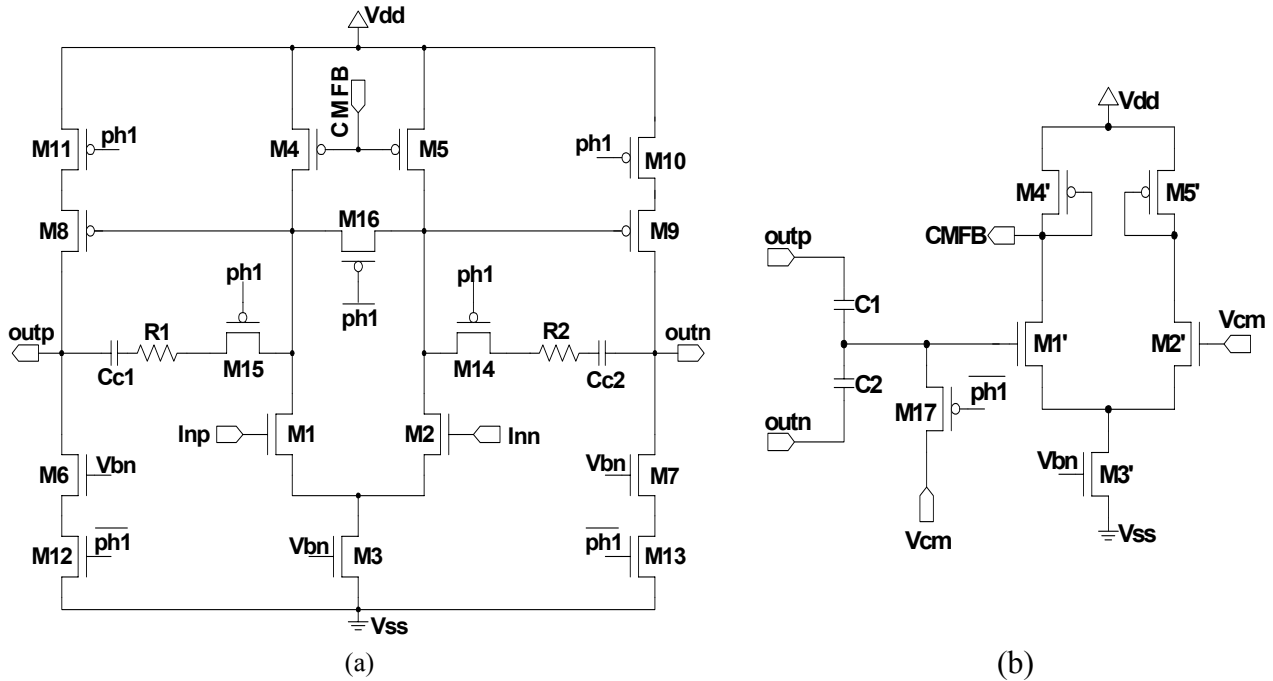


Fig. 4. (a) Fully differential switched opamp. (b) SOA common mode feedback circuit.

The amplifier, employed in the ADC analog core as SOA, is based on a simple two-stage Miller operation transconductance amplifier (OTA) [Fig. 4(a)]. It has a fully differential architecture, mainly to improve power supply rejection ratio (PSRR) and to enhance the signal swing and an active common mode feedback (CMFB) circuit [Fig. 4(b)]. The dissipation is 150 nA for the input stage and 1  $\mu$ A for the output stage (500 nA per branch). This means that the current consumption, excluding CMFB circuit, is 1.15  $\mu$ A during ON phase and 150 nA during OFF phase. In order to produce a 0.5-b redundancy, two comparators (each formed by a preamplifier and an analog latch) have been used in this design, where an input offset sensing (IOS) method is used, where the offset cancellation is performed by closing a unity-gain loop around the preamplifier and storing the offset on the input coupling capacitors [10]. In both the SH and X2 blocks, the auto-zero operation of the amplifier allowed in classical SC architectures cannot occur because, in the sample phase, SOA output is “off”, so this effect results in a huge loss of codes and potential linearity problems. In order to avoid this problem, in the second cycle clock (the first after *ADCsample* “on”), SH inputs are inverted, and at the third cycle clock, normal conditions are restored. So, the offset stored in first time, which at the end of conversion is multiplied with  $2^{N-1}$  ( $N$  = number of bits of the ADC), is subtracted with next offsets (next cycles clocks) that are multiplied with  $2^{N-k}$ , where  $k = 2 \dots 10$  is the number of the cycle clock. This means that, after *ADCsample* is “on”, the residual signal of conversion is inverted: The SUM block needs additional control logic [8].

Let us consider now the ADC timing diagram (Fig. 5). The reset signal asynchronously initializes the digital section of the ADC: the output register is loaded to “0” as a conversion result, but *ADCdav* is low so this is not a really conversion result. An initialization is recommended each time a new data acquisition begins, but, to minimize power supply consumption, the reset pulse width must be as short as possible. In Fig. 5, the acquisition mode (of *data#1* and *data#2*) is “free running”, and

the data stream is collected by a microcontroller which can operate either in edge mode or in level mode. In fact,  $ADC_{dav}$  raises each time that a valid data conversion is available (edge triggered) and remains stable until the ending of a new conversion (level triggered). The ADC starts when it wakes up from stand by condition. The internal state is bounded to rising edge of the clock; an initial start up time allows the analog part to reach a steady state, and then, on the falling edge of the clock the conversion starts (the internal signal  $ADC_{sample}$  is shown for clarity). To process the input value, the ADC takes 10 clock cycles plus an additional clock cycle to reinitialize the internal logic. The data output  $ADC_{out}$  [9:0] is registered, so it is stable until the register is updated. In Table I, a summary of the experimental results of the A/D integrated converter is presented. Dynamic characteristics, such as total harmonic distortion (THD), spurious free dynamic range (SFDR), and equivalent number of bits (ENOB), have been measured using a single-ended input test, leading to a lower value (8.4 b) for ENOB.

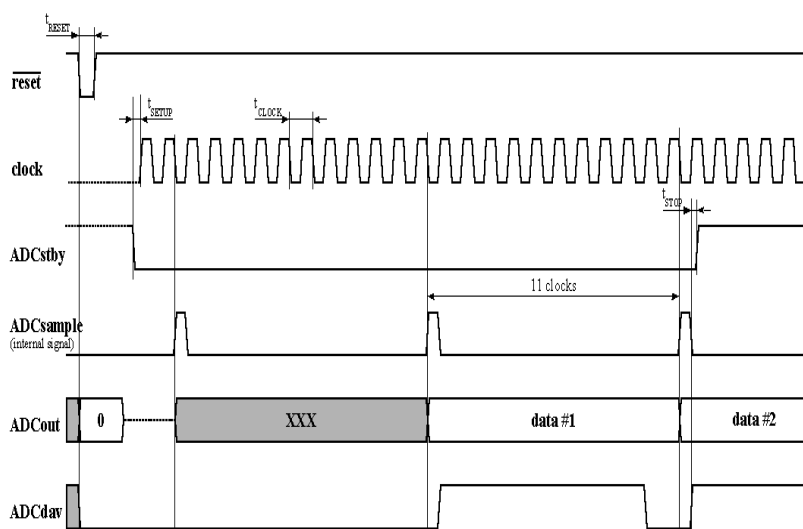


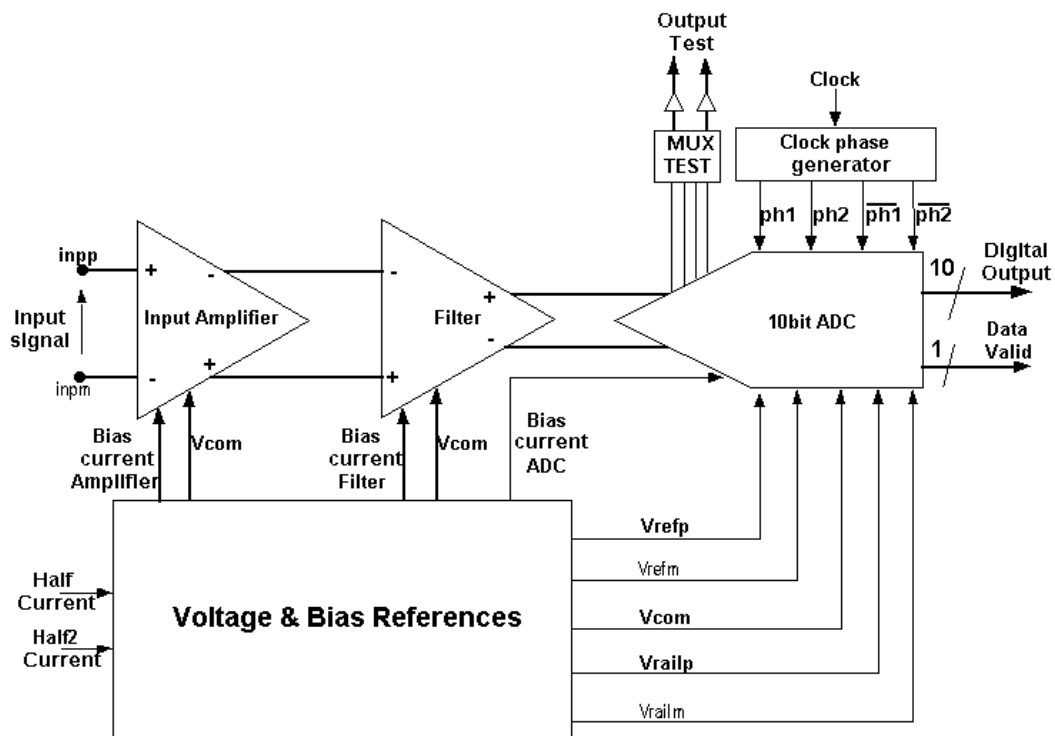
Fig. 5. ADC timing diagram.

TABLE I  
SUMMARY OF THE MAIN ADC PERFORMANCE

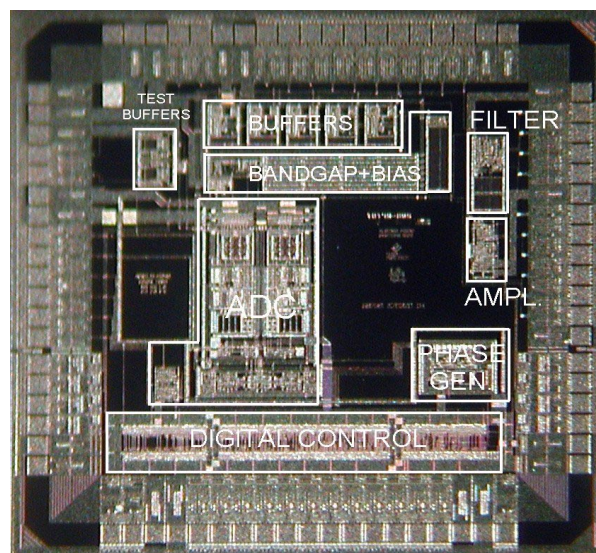
Measurement Condition	Minimum	Typical	Maximum	Unit
Supply voltage	2	2.8	3.5	V
Sampling rate	0.7	2.9	3,6	KS/s
Bias current	1/4 Full	Full	Full	-----
Resolution	10			bit
Consumption (Analog Part)	0.56	2.92	3.9	$\mu$ A
Consumption (Digital Part)	0.67	3.47	4.17	$\mu$ A
INL	1.13	0.98	0.85	LSB
DNL	0.73	0.67	0.75	LSB
Input Noise	0.43	0.42	0.4	mV rms
Offset	0.72	0.73	0.7	mV
THD	56.6	56.3	57.6	dB
SFDR	60.2	59.6	61.1	dB
ENOB	8.4	8.4	8.4	bit
Offset drift	-	21.4	-	$\mu$ V/ $^{\circ}$ C
Gain drift	-	100	-	ppm/ $^{\circ}$ C
Active Area	0.8			mm <sup>2</sup>

The presented ADC has been designed as a part of an ultralow-power signal processor (ULPSP), developed for implantable pacemakers [ASIC schematic representation in Fig. 6(a) and chip microphotograph in Fig. 6(b)]. It has a front-end section, a low-pass filter and the 10-b ADC.

ULPSP includes a bandgap referred to ground, five voltage buffers (showing a total consumption of  $0.775 \mu\text{A}$ ) to provide the proper references for ADC operation, and device common mode operation. The chip is pad-limited and the silicon area could be reduced, without test pads. In fact, the ADC cell area is about  $0.8 \text{ mm}^2$ . The programmability of current generators, which produce a current reduction, is implemented by Half Current and Half2 Current digital pins.



(a)



(b)

Fig. 6. (a) Chip block diagram. (b) Chip photo (die area: about  $9 \text{ mm}^2$ ).

### III. CONCLUSION

In this brief, we have presented a new integrated ADC used in an ULPSP for biomedical applications. The SOA technique here utilized offers good characteristic improvements for ADCs in implantable device applications. We have shown that, with the cyclic conversion algorithm approach, it is possible to achieve a good resolution with ultralow-power consumption and low die area.

## REFERENCES.

- [1] A. Baschiroto, R. Castello, and F. Montecchi, "Design strategies for low-voltage SC circuits," *Electron. Lett.*, vol. 30 no. 5, pp. 378-380, Mar. 1994.
- [2] J. Crols, M. Steyaert, and W. Sansen, "Switched op-amp: an approach to realize full CMOS SC circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol.29, pp.936-942, Aug. 1994.
- [3] A. Baschiroto and R. Castello, "A 1V 1.8 MHz MOS switched-opamp SC filter with rail-to-rail output swing," in *Proc. ISSCC Conf.*, San Francisco, CA, 1997, pp. 58-59.
- [4] V. Peluso, P. Vancorenland, M. Stayaert, and W. Sansen, "900 mV differential class AB OTA for switched op-amp applications," *Electron. Lett.*, vol. 33, no. 17, pp. 1455-1456, Aug. 1997.
- [5] G. Ferri, A. Costa, and A. Baschiroto, "A 1.2V rail-to-rail switched buffer topologies," in *Proc. ICECS*, Lisboa, Portugal, Sept. 1998, pp. 45-48.
- [6] G. Ferri, and A. Baschiroto, "Low-voltage rail-to-rail switched buffer topologies," *Int. J. Circuit Theory Applicat.*, vol. 29, no. 4, pp. 413-422, July 2001.
- [7] A. Gerosa, A. Novo, and A. Neviani, "Low-power sensing and digitization of cardiac signals based on sigma-delta conversion," in *Proc. ISPLED*, Rapallo, Italy, Sept. 2000, pp. 386-389.
- [8] B. Ginetti, P. G. A. Jespers, A. Vandemeulebroecke, "A CMOS 13-b Cyclic RSD A/D Converter", *IEEE J. Solid-State Circuits*, vol. 27, pp. 957-964, July 1992.
- [9] M. Waltari, K. Halonen, "1-Volt 9-bit Pipelined CMOS ADC," in *Proc. ESSCIRC*, 2000, pp. 360-363.
- [10] B. Razavi, and B. A. Wooley, "Design Technique for High-Speed, High-Resolution Comparators," *IEEE J. Solid-State Circuits*, vol. 27, Dec 1992.
- [11] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5 V, 1  $\mu$ W Successive Approximation ADC," in *Proc. ESSCIRC*, Florence, Italy, Sept. 26, 2002, pp. 247-250.