

RAD-HARD ASIC FOR PHOTODETECTOR SIGNAL PROCESSING

F. Brandani⁽¹⁾, S. Chicca⁽²⁾, S. Puccini⁽¹⁾, M. Stagi⁽¹⁾

⁽¹⁾ Galileo Avionica – a Finmeccanica S.p.A. Company – Space Equipment Business Unit
Via A. Einstein 35, 50013 Campi Bisenzio (FI), Italy
Email: fabio.brandani@officine-galileo.finmeccanica.it
Tel. +39 055 8950704 - Fax: +39 055 8950613

⁽²⁾ Aurelia Microelettronica S.p.A.
Via Giuntini 25 – 56023 – Navacchio (PI) – Italy

Abstract - A front-end ASIC designed to collect signals from CCD or CMOS photodetectors allows the realization of a compact and low-power data acquisition system, performing analogue processing and digitization. In the design of the device, fabricated using a Rad-Hard technology, several solutions have been used, both in the digital and in the analogue section, to improve the performance and to reduce the susceptibility to single event effects. The paper describes the chip design and the experimental characterization of the prototypes before and after radiation tests.

Index terms — Analog-to-digital conversion, CCD, BiCMOS analog integrated circuits, Digital-to-analog conversion, Front-end, Photodetectors, Radiation hardness, Testing.

Introduction

In the frame of a Earth observation program of the Italian Space Agency, Galileo Avionica has been involved in some technological studies devoted to finalize the design of a high resolution hyperspectral camera. One of the major tasks of this study was the development of high integration electronics blocks with the necessary speed for the acquisition and processing of large amounts of data, as needed in a hyperspectral camera. In addition, the possibility to use the same front-end electronics also for instruments and attitude sensors operating in severe radiation environment, has pushed to a design employing radiation hardened technology.

In this frame, a new mixed signal ASIC for detector signal conditioning, sampling and digitization has been realized (SSP: Sensor Signal Processor) with the collaboration of Aurelia Microelettronica.

The SSP has been developed in order to fulfil the requirements of high pixel rate (up to 5MSPS) and of unchanged EOL performance after exposure to high radiation dose (>300 krad(Si)).

Besides, the SSP design is in line with the trend to reduce the size, weight and power consumption of digital imaging sensors and electronics for spaceborne systems. In fact, the SSP can be used to replace about 100 discrete components, with a great reduction in PCB occupied area (about 15X), weight (about 5X) and power consumption (about 2X).

To obtain a high immunity to TID, the component has been realised using ATMEL DMILL technology (Total Dose ≥ 1 Mrad nominal, latchup free).

Moreover, several design solutions have been used, both in the digital and in the analog section, to minimize the radiation induced effects on the device.

Architecture

The block diagram of the SSP is reported in figure 1. The main functions needed to perform analogue processing and digitization of signals outgoing a photodetector (visible and/or infrared) can be seen in the upper part of the block diagram. A CDS channel is provided to be used with CCD detectors, while 7 High Speed Sample and Hold channels are provided for CMOS detectors, like visible APS or visible and IR hybrid devices. These channels can also be used to process and convert housekeeping (HK) signals.

All the channels are equipped with a Programmable Gain Amplifier (x1 – x4) and with an offset adjustment input. A multiplexer stage selects one of the 8 channels to be converted with 12 bits resolution. The input range of the ADC is 3V, hence the overall system gain is about 0.73 mV/LSB when the PGA gain is set to 1 and about 0.18 mV/LSB when the PGA gain is set to 4.

A 6 bits Hamming code is provided together with the output to improve data transmission reliability.

A 12 bits general purpose D/A converter is also integrated in the device.

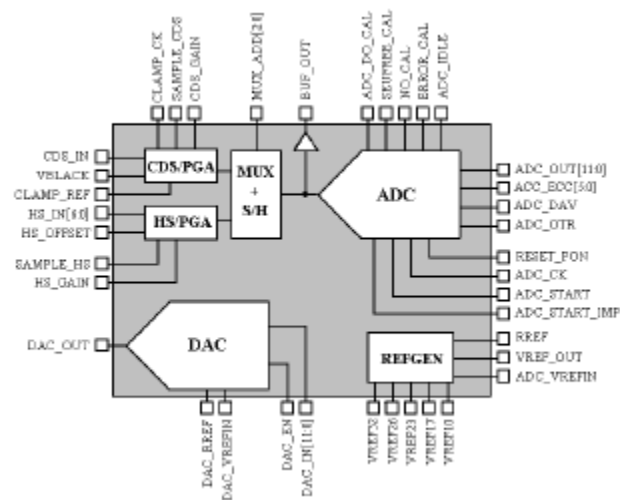


Fig. 1 – SSP ASIC functional block diagram

The ADC is a digital self-calibrated 2 bit/stage pipelined converter. The total number of stages is 15 and the number of effective bits is 16, but only 12 bits are available at the output while the remaining 4 bits are used for the digital calibration.

More in detail, each pipe-stage is constituted by a low-resolution 2 bit coarse sub-ADC, a 2 bit sub-DAC, and an interstage residue amplifier. Sub-DAC and residue amplifier in each stage are merged in a unique circuit called MDAC (Multiplying DAC).

A block diagram of the ADC is reported in figure 2.

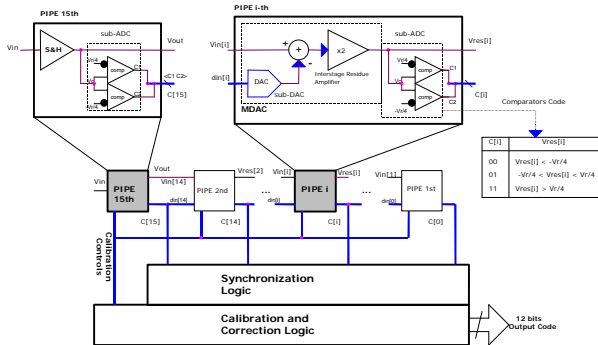


Fig. 2 – ADC functional block diagram

A key issue in the ADC is represented by the incorporation of a digital self-calibration and correction mechanism for reducing (ideally eliminating) the impact of non-linearity effects.

The goal of digital-error correction is to eliminate the effects that non-idealities in the sub-ADCs have on the overall converter operation. Since non-idealities in a stage can cause over range problems for the next stage, correction approaches are based on including 1 bit of redundancy to eliminate these problems. This is achieved storing the effective value of the MDAC (coefficients) levels in a look up table (LUT); these values are obtained by means of an opportune procedure, averaging the results of MDAC value conversion for 2^{16} steps. In this application, calibration is applied only to the 6 first stages.

The use of this calibration/correction scheme is also useful to absorb the negative influence of failures and errors caused by radiation effects.

As far as the DAC is concerned, a variable step current (4096 uniformly distributed values from 0 to about 3.2 mA) is supplied to an external pad. An external resistor connected to ground is needed to convert this current to an adjustable voltage. This feature can be useful, for example, to generate programmable voltages for the analog channels offset compensation.

Two foundry runs have been already performed. In the first run 20 prototypes have been produced and subsequently tested by Galileo Avionica. On the basis of the results of this first test campaign, some modifications have been incorporated in the design to improve the device performances. Particularly, the input stage of the HS channels has been modified to make it differential and the digital part of the device

has been modified to make it compatible with 3.3V supply. Moreover, some layout modifications have been made to adapt the chip to the flight package and a second foundry run has been performed. The design is now in compliance with the ATMEL layout rules and it is ready for flight procurement.

Some samples of the 2nd foundry run can be seen in figure 3.

The main features of the SSP are resumed below:

- 3V input range
- 5V analogue supply; 3.3V or 5V digital supply
- 12-Bit 5 MSPS self calibrating A/D converter
- 12-Bit 1 μ S D/A converter
- Internal Voltage Reference generator
- 1 integrated CDS channel with programmable gain amplifier (PGA, X1 – X4) and offset adjust
- 7 High Speed S/H channels with programmable gain amplifier (PGA, X1 - X4) and offset adjust
- 8:1 Multiplexer
- 12 bit output with 6 bit Hamming code
- Low power consumption: 500 mW max
- Extended Temperature Range
 - Components fully tested from -40°C to $+80^{\circ}\text{C}$
- RH Device:
 - Total Dose $\geq 1\text{Mrad}(\text{Si})$
 - Designed to tolerate 10^{14} neutrons/cm²
 - SEU tolerance $\geq 70\text{MeV/mg/cm}^2$
 - Latchup free

Design Main Features

Several design techniques, both in architecture and in layout, have been used to improve the radiation robustness of the SSP. As an example, the following tricks have been used in the design:

- A triple redundancy with majority vote logic circuit protects the digital registers against Single Event Upset.
- The design has been carried out using SOI technology, that allows to form devices in insulated areas, which show no noticeable leakage current as effect of the total dose and are implicitly latch-up free.



Fig. 3 – SSP samples (2nd run)

Moreover, the SSP is designed for fully digital testability. Some test structures such as a Scan Chain and BIST help to observe the internal digital nodes and increase the reliability for aerospace applications.

For debugging purposes, with these auxiliary internal test structures it is possible:

- To provide a direct signal to the Sample and Hold block, bypassing the front end;
- To provide a differential ADC input signal from external sources;
- To provide the buffer input signal from external sources and monitoring the first ADC stage output externally.

Furthermore, the digital part of the ADC is provided with one scan chain for the test.

To minimize the effects of eventual errors in the ADC output or in the transmission, a 6 bit Hamming code is provided. Using this code it is possible to correct a 1 bit error on ADC output code and to detect a 2 bit error.

Testing

The test equipment used for the characterization of the SSP can be seen in figure 4.



Fig. 4 – SSP Test Equipment

The equipment is based on a PC with some I/O boards, an external arbitrary waveforms generator, a programmable 8 channels power supply, a low distortion waveforms generator, 3 multimeters and an oscilloscope. Moreover, an appropriate PCB has been developed to house the device under test and to provide it with the required stimuli. All the instruments are controlled by the PC, that is used also to acquire the outputs from the device and to process them. A SW with opportune procedures has been developed to perform automatically all the test sequences.

A total number of 14 chips have been tested at 20°C, while 6 chips have been tested over a temperature range from -40°C to +80°C. Subsequently, these 6 chips have been irradiated with different levels of total dose using a Co-60 γ source. All the radiation testing of the chips has been performed according with ESA/SCC 22900. The dose rate has been set to 36 krad/hour for all the devices. As far as the total dose is concerned, 2

chips have been irradiated up to a total dose of 50 krad, 2 chips have been irradiated up to a total dose of 100 krad and the other 2 chips have been irradiated up to a total dose of 300 krad. All the devices were switched on and clocked during the irradiation. A first test campaign has been performed immediately after the end of the irradiation. Subsequently, the devices have been backed for 168 hours at 100° and a second test campaign has been performed. Both these test campaigns have been performed with components at a temperature of 20°C.

Performance

Some of the main results of the pre-irradiation testing are reported in Table 1 and Table 2. All the shown values have been obtained with the PGA gain set to 1.

SECTION	-40°C	+20°C	+80°C	Units
POWER				
Dig. section	7	7	7.16	mW
An. section	461.2	472.5	479.7	
ADC_INL	1.24	1.07	1.05	LSB
ADC_DNL	0.4	0.4	0.38	LSB
HS Input Referred Noise	0.4	0.42	0.42	mV
CDS Input Referred Noise	1.7	1.4	1	mV

Table 1 – Main pre-irradiation test results (3MHz conversion frequency)

SECTION	-40°C	+20°C	+80°C	Units
POWER				
Dig. section	12	12.37	12.54	mW
An. section	470	475	487	
ADC_INL	1.88	1.66	1.56	LSB
ADC_DNL	0.4	0.4	0.38	LSB
HS Input Referred Noise	0.4	0.4	0.42	mV
CDS Input Referred Noise	1.4	1.5	1.3	mV

Table 2 – Main pre-irradiation test results (5MHz conversion frequency)

As it can be seen from table 1 and 2, no significant variation in the performances has been observed with temperature variation from -40°C to +80°C. It has to be noted that, as far as the input referred noise is concerned, the measurements have to be considered

as conservative. In fact, due to the great complexity of the test equipment, all the tests have been performed in a quite noisy environment, that caused some problem especially for the CDS channel.

All the pre-irradiation measurements performed on the devices have been repeated after the irradiation. The post irradiation tests show a good immunity of the devices to TID. In fact, no significant change in the performances has been highlighted after a total dose of 300krad. Some of the main results of the post-irradiation tests, compared with the results of the relevant pre-irradiation tests, are reported in Table 3 and Table 4.

SECTION	Pre-irr.	Post-irr.	After annealing	Units
POWER				
Dig. section	12.6	13.4	13.4	mW
An. section	472	471	470	
ADC_INL	1.7	1.7	1.8	LSB
ADC_DNL	0.38	0.37	0.32	LSB
HS Input Referred Noise	0.4	0.45	0.42	mV
CDS Input Referred Noise	1.7	1.6	1.6	mV

Table 3 – Main post-irradiation test results compared with the relevant pre-irradiation ones for chip # 5 (5MHz conversion frequency, 300krad TID, T=20°C)

SECTION	Pre-irr.	Post-irr.	After annealing	Units
POWER				
Dig. section	12.1	13.4	13.4	mW
An. section	477	475	473	
ADC_INL	1.25	2.18	2.26	LSB
ADC_DNL	0.36	0.36	0.35	LSB
HS Input Referred Noise	0.4	0.42	0.42	mV
CDS Input Referred Noise	1.5	1.7	1.7	mV

Table 3 – Main post-irradiation test results compared with the relevant pre-irradiation ones for chip # 7 (5MHz conversion frequency, 300krad TID, T=20°C)

Only the results relevant to the chips irradiated up to 300krad are highlighted, since no changes at all were observed in the performances of the components irradiated with lower levels of total dose.

As it can be seen by table 3 and table 4, no significant changes in the performances occurred after a total dose of 300krad. The only noticeable effect is a slight increase in ADC INL for chip #7. In the following figures it is possible to see chip #7 ADC INL before and after irradiation.

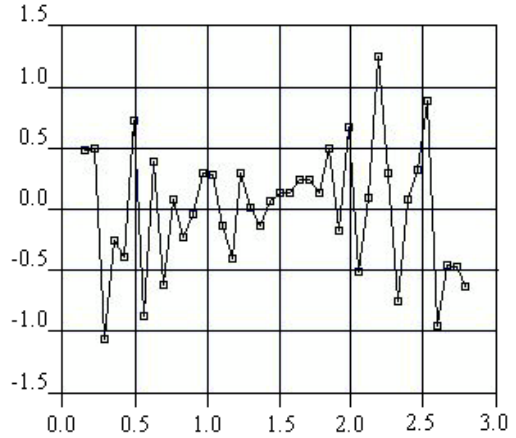


Fig. 5 – Chip #7 ADC INL vs input voltage before irradiation

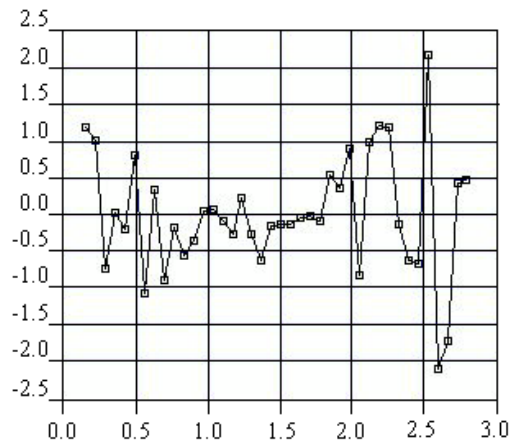


Fig. 6 – Chip #7 ADC INL vs input voltage after irradiation (300krad total dose)

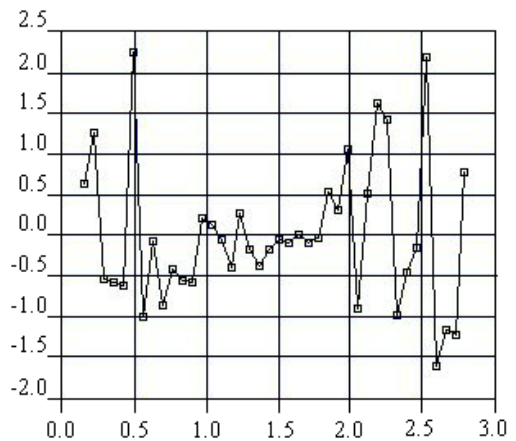


Fig. 7 – Chip #7 ADC INL vs input voltage after irradiation and annealing (300krad total dose, 168 hours at 100°C)

As it can be seen in figures from 5 to 7, the maximum value of INL has slightly increased, but on average the ADC INL has remained almost unchanged after the irradiation.

Moreover, it is interesting to notice that the ADC has no missing codes, both before and after irradiation, thanks to its calibration circuit.

As a conclusion, it is possible to say that the tested components showed a good immunity to TID up to a level ≥ 300 krad, and that the SSP can be considered suitable to be used in severe radiation environments and in aerospace applications.

Conclusions

SSP, a signal processor for CCD or CMOS photodetectors to be used in severe radiation environment and aerospace applications, is presented in this paper. It collects data from external sensors and processes them before digitization.

The front-end electronics has a CDS and 7 high-speed Sample/Hold input channels, all with programmable gain between 1 and 4.

The internal 12 bit pipelined ADC can be used up to 5Msamples/s and is guaranteed from missing codes.

A self-calibration function allows to minimize (ideally eliminate) all non-linearity effects due to internal components mismatch.

A general-purpose 12-bit 1 MHz current DAC is implemented and can be used for offset corrections.

SSP is designed in order to maintain his functionality and performance in space environment and to withstand TID > 1 Mrad. The device is SEL free, and it has a SEU tolerance > 70 MeV/mg cm².

Several auxiliary structures make easier to observe internal states and signals in the chip, during its normal functionality and greatly improve its reliability.

All the tests performed on the prototypes show the functionality of the design and the validity of the techniques applied to improve the radiation immunity of the component.

Acknowledgements

The authors of this paper represent all the people involved in the design and development of this component. In particular, we would like to mention Luca Colombini, Cristian Garbossa, Simone Giovannetti, Franco Bigongiari, Maurizio Lippi and Andrea Brogna for their contribution to the development of the device and Andrea Dell'Immagine for his contribution to the development of the test equipment.

References

- [1] P. Bellandi, F.Brandani, A. Brogna, S. Chicca, L. Colombini, C. Garbossa, S. Puccini, R. Saletti, M. Stagi, "A 12-bit pipelined self-calibrated radiation hardened ADC for aerospace applications", to be published in Proceedings of RADECS 2002, September 19-20, 2002, Padova, Italy.
- [2] Rudy J. Van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer 1994.
- [3] Andrew N. Karanicolas, Hae-Seung Lee, Kantial L. Bracania, "A 15-bit 1-Msample/s Digitally Self Calibrated Pipeline ADC", IEEE J. Solid State Circuits, Vol. 28, Dec 1993.
- [4] Eric G. Soensen, Randall L. Geiger, "An Architecture and an Algorithm for Fully Digital Correction of Monolithic Pipeline ADC's" IEEE Trans. Circuits Syst.II, vol 42, Mar 1995.
- [5] K. Nagaraj, "Area efficient Self-Calibration Technique for Pipelined Algorithmic A/D Converter", IEEE Trans. Circuits Syst. II, Vol 43, July 1996.
- [6] João Goes, João Vital, Jose E. Franca, "Systematic Design for Optimization of High Speed Self Calibrated Pipeline A/D Converters", IEEE J. Solid State Circuits, Vol. 45, Dec 1998.
- [7] D. Labate, F. Svelto, "Development of critical technologies for the COSMO/Skymed Hyperspectral Camera", Proceedings of RTO SET Symposium on "Space-Based Observation Technology", Island of Samos, Greece, 16-18 October, 2000, RTO-MP-61.
- [8] A. Bini, F. Brandani, M. Brotini, C. Caprini, R. De Vidi D. Labate, A. Romoli, M. Stagi, L. Tommasi, V. De Cosmo, "Hyperspectral Earth Observer (HYPSEO) Program", Proceedings of 52nd International Astronautical Congress, Toulouse, France, 2001, October 1-5.

Contacts

Technical:
fabio.brandani@officine-galileo.finmeccanica.it

Commercial:
massimo.lucarini@officine-galileo.finmeccanica.it

URL:
www.spazio.galileoavionica.it