

# A 12-bit pipelined self-calibrated radiation hardened ADC for aerospace applications

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**Abstract** – A front-end ASIC chip designed to collect signals from CCD or CMOS photodetectors allows the realization of a compact and low-power data acquisition system performing analogue processing and digitalization. The device has been fabricated in Rad-Hard technology and several design solutions have been used, both in the digital and in the analogue section, to improve the performance and to reduce the susceptibility to single event effects. The paper describes the chip design and the experimental characterization of the prototypes before and after radiation tests.

**Index terms** — Analog-to-digital conversion, radiation hardness, SOI, testing.

## I. INTRODUCTION

This work describes an ASIC chip, designed and developed for Galileo Avionica, which is used in their front-end electronics and to operate in a severe radiation environment. A Sensor Signal Processor (SSP) collects data from 8 different sources: one a CMOS image sensor system based on a Charge Coupled Device (CCD) and 7 high speed sample/hold channels for signals coming from CMOS photodetectors or from other instrument sub-units.

The challenge is to achieve an unchanged end-of-life performance after exposure to high radiation dose (>100 krad (Si)): several special design techniques, used both in the architecture and in the chip layout, and a latch-up free BiCMOS / SOI technology suitable for aerospace applications assure a total dose of 1 Mrad and a Single Event Upset (SEU) tolerance of 70 MeV / (mg cm<sup>2</sup>).

The chip is available from Galileo Avionica in a 132 MQFP\_F package, and operates from a single +5V analog supply and a +5V/+3.3V digital supply.

## II. ARCHITECTURE

A block diagram of chip architecture is shown in Fig. 1, where four sub-sections are recognizable: a front-end, an ADC, a DAC and a reference block.

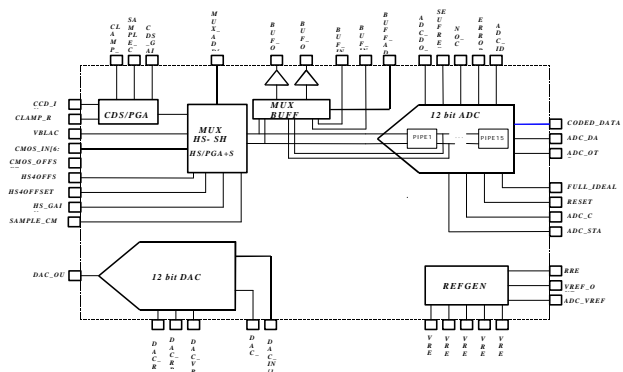


Fig. 1. Architectural diagram of SSP chip

The first one is the interface to the external input sensors, the signals of which are conditioned and pre-processed before quantization. The ADC is a pipelined converter because of high-speed requirements. Moreover, a 12 bit DAC compensates the channel offset to maximize performance. Then, the reference generator supplies all voltages and currents for the rest of the circuit

### A. Front End

The Front-end is the interface between the sensors and the converter, used to condition the input signals. It deals with a Correlated Double Sampling (CDS) stage, with programmable gain 1 or 4, used to amplify CCD sensor outputs, and a 7 input High Speed (HS) stage with the same programmable gain 1 or 4, connected to CMOS sensor outputs. The HS stage is also used as Sample and Hold stage (S&H), with the additional

function of transforming the single ended CDS output into a differential input for the ADC.

The internal multiplexer output voltage and the output voltage of the ADC first stage are buffered and carried out of the chip for measure purposes without altering the normal functionality during the chip test.

### B. ADC and calibration

The ADC [1, 2] is a digital self-calibrated 2 bit / stage pipelined converter: as result of conversion, 2 bit are at the output of two comparators. The number of stages is 15, so the number of effective bits is 16 but only 12 bits are available at the output while the remaining 4 bits are used for the digital calibration.

The functional structure of a pipelined ADC is shown in Fig. 2. The converter is a cascade of 15 stages, each one contributing to the output code with 1 bit. More in detail, each pipe-stage has a low-resolution 2 bit coarse sub-ADC, a 2 bit sub-DAC, and an interstage residue amplifier.

SubDAC and residue amplifier in each stage are merged in a unique circuit called MDAC (Multiplying DAC). A key issue in pipelined ADCs is that they rely on the incorporation of a mechanism for reducing (ideally eliminating) the impact of the non linearity effects as well as those from any other error source by a self-calibration and correction scheme, which is totally digital.

Calibration techniques [3, 4, 5] are mainly aimed at reducing effects caused by component mismatch and gain errors in the MDACs. In this application, the calibration is performed only on the first 6 stages and it is executed by compensating mismatch in the MDAC of the stage under calibration.

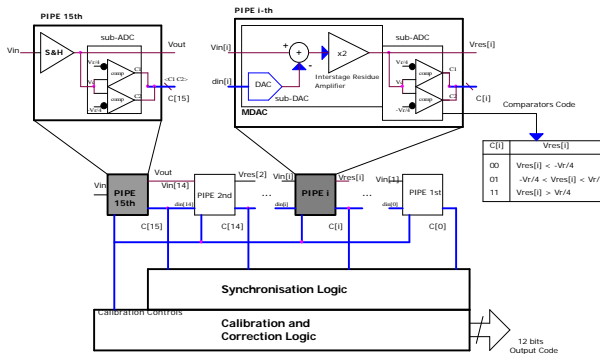


Fig. 2. Functional description of the pipelined ADC

On the other hand, the goal of digital-error correction is to eliminate the effects that non-idealities in the sub-ADCs determine on the overall converter operation. Since non-idealities in a stage cause over range problems for the following one, correction approaches are based on the inclusion of 1 bit of redundancy to eliminate these problems. This is achieved storing in a look up table (LUT) the effective values of the MDAC (coefficients) levels for the stages that have to be calibrated. The LUT is filled using the remaining stages of the ADC.

An interesting issue of this implementation is the use of this calibration / correction scheme to absorb the negative influence of failures and errors caused by radiation effects.

### C. DAC

The DAC supplies a variable step current (4096 uniformly distributed values) to an external pad. An external resistor connected to ground converts this current in an adjustable voltage which can be used as a programmable offset compensation for the analog channel.

### D. Reference generator

Several reference sources are internally available: a band gap voltage generator provides all voltage and currents to supply other sub blocks. However, it is possible to exclude the on-chip reference and connect a more stable external one.

A power-off pulse at start-up (1  $\mu$ s min.) is mandatory to guarantee the proper functionality of internal bandgap voltage generator.

External storage capacitors are also used to satisfy the demand of current peaks from internal circuitry.

## III. DESIGN FEATURES

Some special design techniques, both in architecture and in layout, has to be used to greatly improve the robustness of the SSP against radiation degradation.

A triple redundancy with majority vote logic circuit protects the digital registers against Single Event Upset (SEU), while the analogue part is designed without using edgeless MOS transistors because the SOI technology allows to form devices in insulated areas which show no noticeable leakage current as effect of the total dose.

A clever expedient to get an error proof code from ADC output is a special encoding: a 6 bit Hamming code can correct a 1 bit error on ADC output code and detect a 2 bit error.

Moreover, the SSP is designed for fully digital testability, some test structures such as a Scan Chain and BIST help to observe the internal digital nodes and increase the reliability for aerospace applications.

For debugging purposes, with these auxiliary internal test structures it is possible:

- To provide a direct signal to the Sample and Hold block, bypassing the front end;
- To provide a differential ADC input signal from external sources;
- To provide the buffer input signal from external sources and monitoring the first ADC stage output externally.

Furthermore, the digital part of the ADC is provided with one scan chain for the test.

### A. ADC direct input.

Two external pins allow to directly access ADC inputs; the signal provided must be fully differential, with common mode equal to the ADC reference voltage (typ

2.5V). The signal is sampled on the falling edge of the clock and the digital output will be available after a latency of 15 clock cycles.

### B. Output buffer programming

The buffer can be used for monitoring the Sample / Hold output and the output of the first stage of ADC. An analog multiplexer selects one of the signals from the front-end electronics. A power down mode is available.

### C. Digital Test

The digital test features introduced in the ASIC are the following:

- *LUT Full-scan*: it is possible to initialize the LUT so the digital part starts from a well-known and consistent state. Forcing from the outside the values of the LUT should be helpful in the case of a malfunctioning of the calibration procedure;
- BIST for complete test of the memory
- Full-scan for the significant flip-flops in order to reach a coverage at least of 96%.

## IV. PERFORMANCES

The chip was fabricated in a 0.8 $\mu$ m single poly 2 metal BiCMOS technology, which is build on bulk SOI substrate (thick SOI). Active and passive devices are in a 1.2 $\mu$ m thick epitaxial layer, on buried oxide layer (400 nm thick) and on a p-silicon substrate.

An interesting feature of this process is the possibility to form devices in several trench-separated zones, not only to improve noise and cross-talk performances but also to minimize the leakage current due to total dose effects.

Two foundry runs have been performed. In the first 20 prototypes have been produced and tested in Galileo.

On the basis of the results of this test campaign, the design was modified to optimize performance and a second foundry run was fabricated. At present, the samples of the second run device have been received and tested with good results, as shown in Tab. 1, over a temperature range from -40°C to +80°C, before irradiation.

	-40°C	+20°C	+80°C
ADC INL [LSB]	$\pm 1.7$	$\pm 1.5$	$\pm 1.5$
ADC DNL [LSB]	0.42	0.39	0.39
HS Input referred Noise [LSB]	1.2	0.9	0.8
CDS Input Referred Noise [LSB]	2	2	1.9
Power Consumption [mW]	480	490	500

Tab. 1. SSP features before irradiation (1 LSB = 700  $\mu$ V)

## V. RADIATION TEST

The used SOI technology is radiation tolerant until 1 Mrad and no changes happen in devices at lower rate: for this application a maximum total dose of 300 krad was required. Special worst case device models with degraded performance are provided in the design kit, in order to simulate the effects of a total dose greater than 1 Mrad.

Some chips are under test and a full characterization is not available yet, but some interesting results coming from preliminary tests are reported in Fig. 3, Fig. 4, Fig. 5 and Fig 6.

These plots show the Integral Non Linearity (INL) of the ADC, measured in LSB, at three different temperatures (-40 °C, 20 °C and 80 °C) versus the same input signal range 0-3 V and the programmable gain is set to 1. The INL is  $\pm 1.7$  LSB, with minimal differences over the temperature range.

The dose rate was 36 krad/h, some tests shows small changes in INL values (2.18 LSB) and offset (3.08 mV). After annealing at 100 °C for 168 h, INL changed to 2.26 LSB and offset to 3.93 mV. The chip test performances are guaranteed for space applications. It is interesting to verify that ADC has no missing code because of calibration circuit, before and after irradiation.

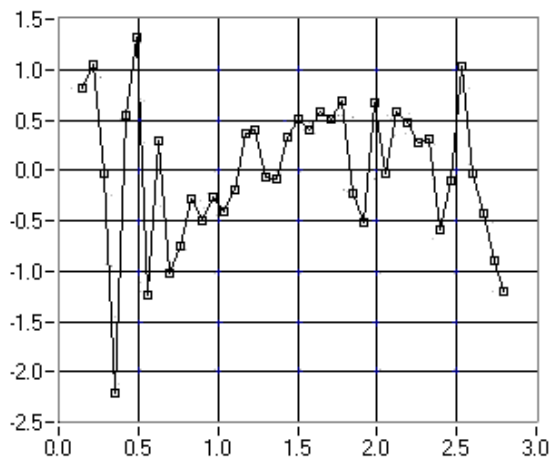


Fig. 3. Pre Irradiation INL versus input signal (@ t=-40°C, Programmable gain = 1)

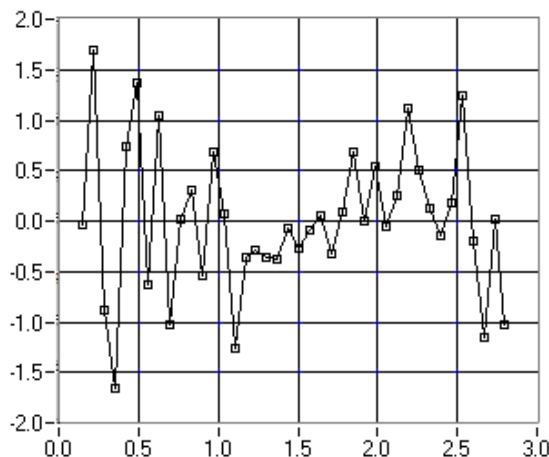


Fig. 4. Pre Irradiation INL versus input signal (@ t=20°C, Programmable gain = 1)

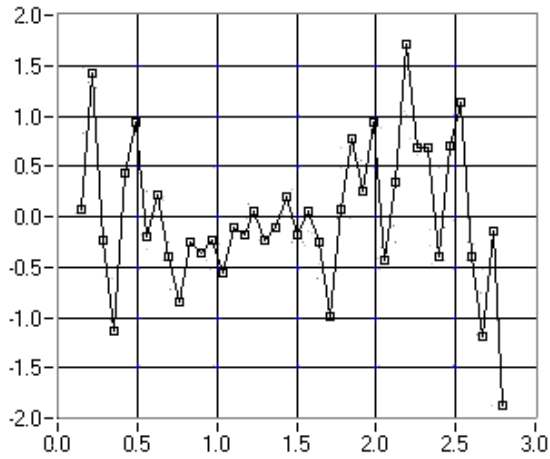


Fig. 5. Pre Irradiation INL versus input signal (@  $t=80^{\circ}\text{C}$ , Programmable gain = 1)

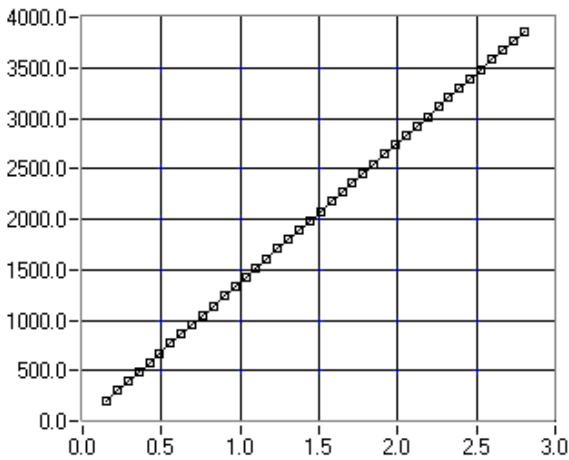


Fig. 6. Output codes versus input signal: because of calibration, there are no missing code before and after irradiation.

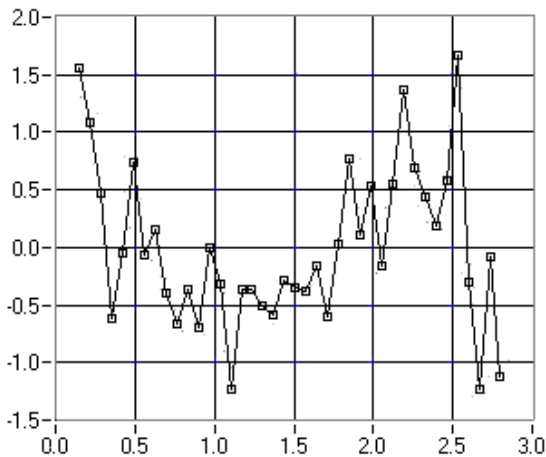


Fig. 7. Post Irradiation INL versus input signal (@  $t=20^{\circ}\text{C}$ ; Programmable gain = 1, total dose = 300 krad)

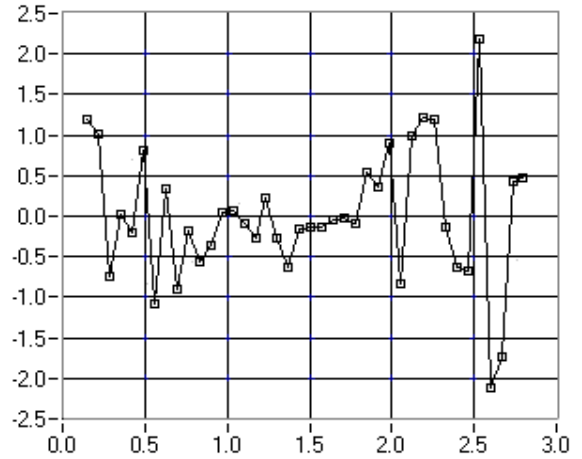


Fig. 8. Post annealing INL versus input signal (@  $t=20^{\circ}\text{C}$ ; Programmable gain = 1, after  $100^{\circ}\text{C}$  for 168 h)

## VI. CONCLUSIONS

SSP, a signal processor for CCD to be used in severe radiation environment and aerospace applications, is presented in this paper. It collects data from external sensors and conditions them before digitalization. The front-end electronics has a CDS circuit and 7 high-speed channels, with programmable gains.

The internal 12 bit ADC is pipelined and self-calibrated, runs to 5 Msamples / s and is guaranteed from missing codes.

A general-purpose 12-bit 1 MHz current DAC is implemented and can be used for offset corrections.

SSP is designed in order to maintain his functionality and performance in space environment and withstand up to a total dose of 1 Mrad and a SEU tolerance of  $70 \text{ MeV} / (\text{mg cm}^2)$ .

Several auxiliary structures make easier to observe internal states and signals in the chip, during its normal functionality and greatly improve its reliability.

Preliminary tests on the prototypes show the functionality of the design and the validity of the techniques applied to make the chip radiation tolerant.

## VII. REFERENCES

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